SPANSION™ Flash Memory

Data Sheet

September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.

AMD

FUJITSU

FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20876-3E

FLASH MEMORY

CMOS

4 M (512 K × 8) BIT

MBM29F004TC/004BC-70/-90

■ DESCRIPTION

The MBM29F004TC/BC is a 4 M-bit, 5.0 V-Only Flash memory organized as 512 K bytes of 8 bits each. The MBM29F004TC/BC is offered in a 32-pin TSOP (1) and 32-pin QFJ (PLCC) packages. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard MBM29F004TC/BC offers access times between 70 ns and 90 ns allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$) , write enable ($\overline{WE}$) , and output enable ($\overline{OE}$) controls.

The MBM29F004TC/BC is pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

(Continued)

■ PRODUCT LINE UP

Part No.		MBM29F004TC/BC	
		-70	-90
Ambient Temperature (°C)		–20 to + 70	–40 to + 85
Max Address Access Time (ns)		70	90
V_{CC} Supply Voltage		5.0 V ± 10%	
Voltage Consumption (mW) (Max)	Operation	193	
	Erase/Program	275	
	TTL Standby mode	5.5	
	CMOS Standby mode	0.0275	
Max $\overline{CE}$ Access (ns)		70	90
Max $\overline{OE}$ Access (ns)		30	35

FUJITSU

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The MBM29F004TC/BC is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Each sector can be programmed and verified in less than 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin. Any individual sector is typically erased and verified within 1.0 second (if already completely preprogrammed) .

This device also features a sector erase architecture. The sector erase mode allows for sectors of memory to be erased and reprogrammed without affecting other sectors. The MBM29F004TC/BC is erased when shipped from the factory.

The MBM29F004TC/BC device also features hardware sector group protection. This feature will disable both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

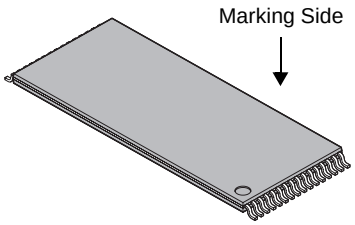
Fujitsu has implemented an Erase Suspend feature that enables the user to put erase on hold for any period of time to read data from or program data to a non-busy sector. True background erase can thus be achieved.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transitions. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7, or by the Toggle Bit I feature on DQ_6 output pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

Fujitsu's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29F004TC/BC memory electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

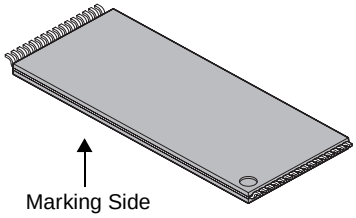
■ PACKAGE

32-pin plastic TSOP (1)



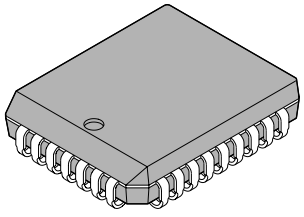
(FPT-32P-M24)

32-pin plastic TSOP (1)



(FPT-32P-M25)

32-pin plastic QFJ (PLCC)



(LCC-32P-M02)

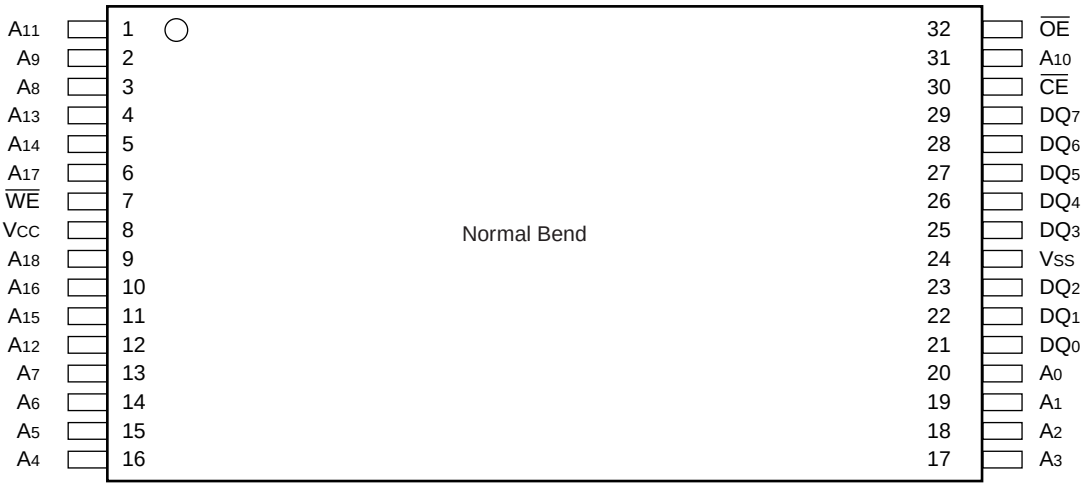
■ FEATURES

- **Single 5.0 V read**, **write**, **and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Pinout and software compatible with single-power supply Flash
  Superior inadvertent write protection
- **32-pin TSOP (1) (Package Suffix : PFTN-Normal Bend Type, PFTR-Reverse Bend Type)**
  32-pin PLCC (Package Suffix : PD)
- **Minimum 100,000 write/erase cycles**
- **High performance**
  70 ns maximum access time
- **Flexible sector erase architecture**
  One 16 K byte, two 8 K bytes, one 32 K byte, and seven 64 K bytes sectors
  Any combination of sectors can be erased. Also supports full chip erase.
- **Embedded Erase™* Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™* Algorithms**
  Automatically programs and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Erase Suspend/Resume**
  Supports reading or programming data to a sector not being erased
- **Sector Protection**
  Hardware sector protect that disables any combination of sectors from write or erase operations
- **Temporary Sector Unprotection**
  Temporary sector unprotection via the command sequence
- **Boot Code Sector Architecture**
- **Fast Programming**
- **Extended Sector Protection**

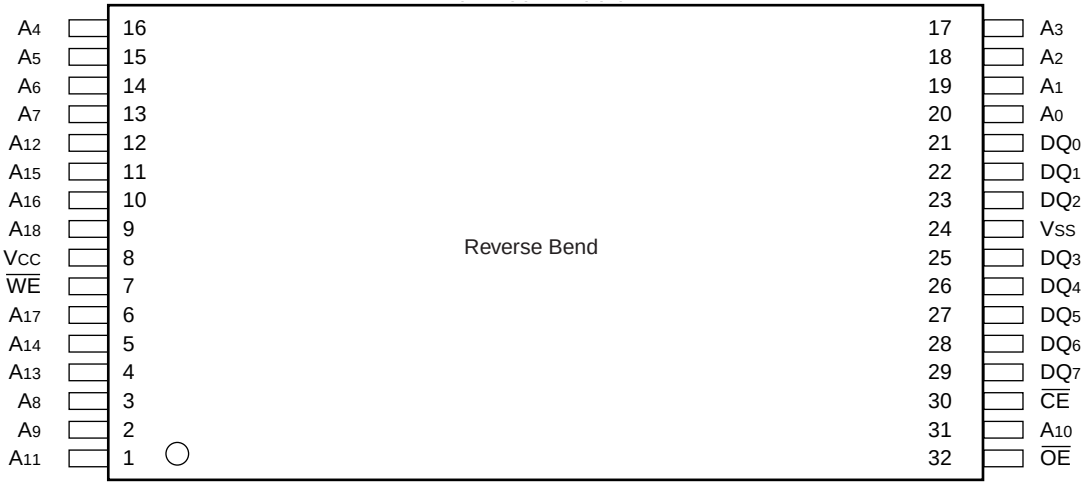
*: Embedded Erase™, Embedded Program™ and ExpressFlash™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENTS

TSOP (1)



(FPT-32P-M24)



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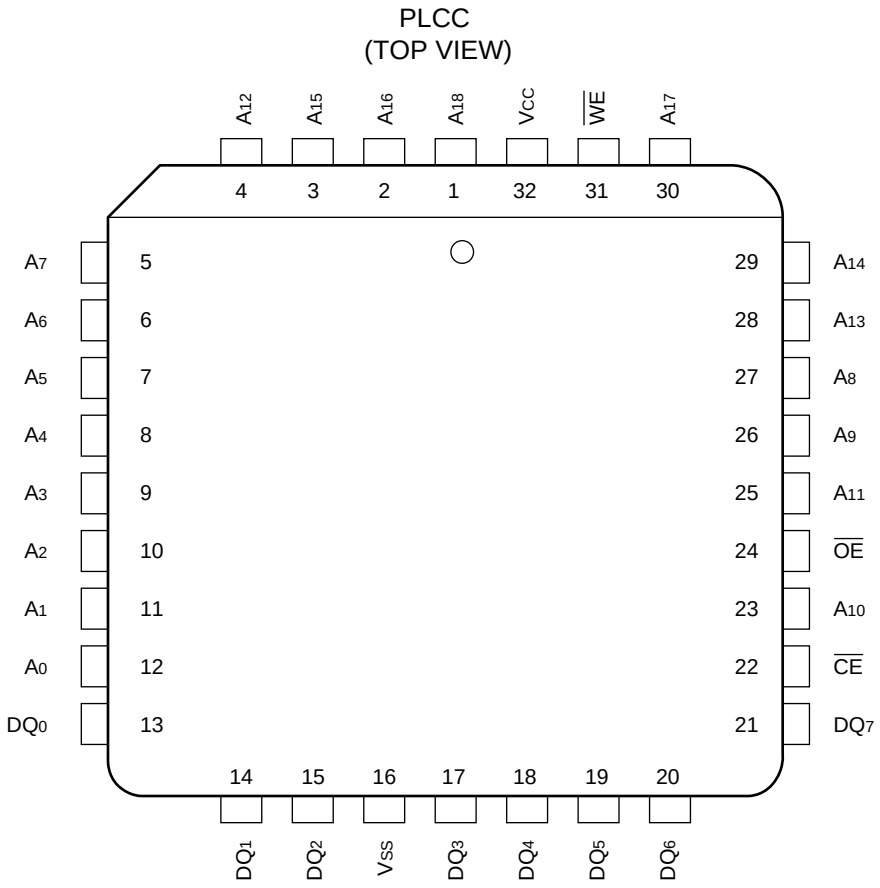


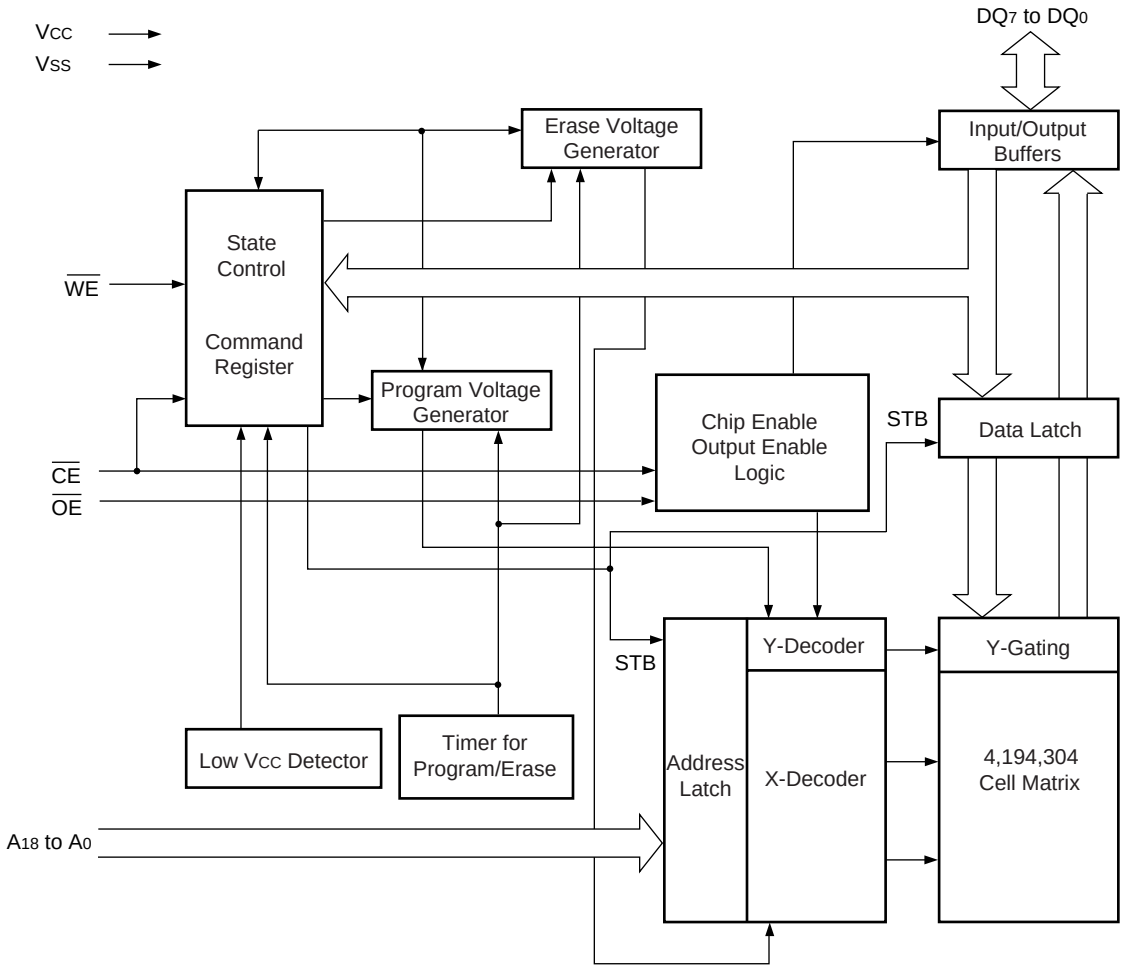
(LCC-32P-M02)

■ PIN DESCRIPTION

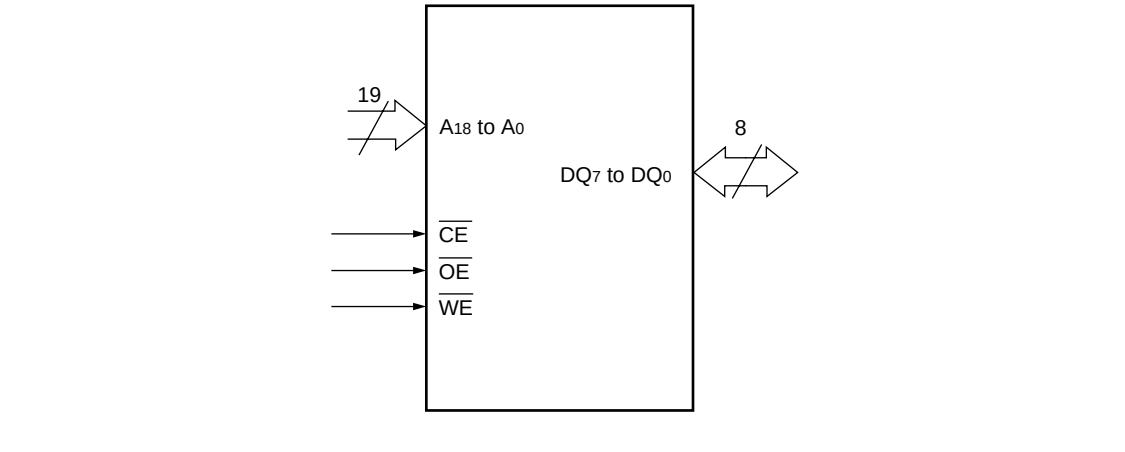
Table 1 MBM29F004TC/BC Pin Configuration

Pin	Function
A_{18} to A_0	Address Inputs
DQ_7 to DQ_0	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable/Sector Protection Unlock
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V±10%)

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

Table 2 MBM29F004TC/BC User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	I/O
Auto-Select Manufacturer Code*1	L	L	H	L	L	L	V_{ID}	Code
Auto-Select Device Code*1	L	L	H	H	L	L	V_{ID}	Code
Read*2	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}
Standby	H	X	X	X	X	X	X	High-Z
Output Disable	L	H	H	X	X	X	X	High-Z
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	D_{IN}
Enable Sector Protection*3	L	V_{ID}	⊓⊔	X	X	X	V_{ID}	X
3-Byte Sector Unlock Sequence	L	V_{ID}	⊓⊔	A_0	A_1	A_6	A_9	D_{IN}
2-Byte Sector Relock Sequence	L	V_{ID}	⊓⊔	A_0	A_1	A_6	A_9	D_{IN}
Command Mode Sector Protect*2	L	V_{ID}	⊓⊔	A_0	A_1	A_6	A_9	D_{IN}
Verify Sector Protect*2, *5	L	L	H	A_0	A_1	A_6	A_9	Code
Hardware Sector Protect*2	H	V_{ID}	L	X	X	L	V_{ID}	X
Verify Sector Protection*2, *6	L	L	H	L	H	L	V_{ID}	Code
Temporary Sector Unprotection*3	L	V_{ID}	⊓⊔	A_0	A_1	A_6	A_9	D_{IN}

Legend : L = V_{IL}, H = V_{IH}, X = “H” or “L”, ⊓⊔ = Pulse Input. See DC Characteristics for voltage levels.

*1 : Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 6.

*2 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*3 : Refer to the section on Sector Protection.

*4 : To activate the command, $\overline{OE}$ has to be taken to V_{ID}.

*5 : In case of Command Mode Sector Protect.

*6 : In case of Hardware Sector Protect.

Table 3 MBM29F004TC/BC Command Definitions

Command Sequence *1, *2, *3	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset *1	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read/Reset Byte *1	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
Auto-Select Manufacture Code	3	555h	AAh	2AAh	55h	555h	F0h	00h	04h	—	—	—	—
Auto-Select Device Code	3	555h	AAh	2AAh	55h	555h	90h	01h	ID	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
Sector Erase Suspend		Erase can be suspended during sector erase with Addr ("H" or "L") , Data (B0h)											
Sector Erase Resume		Erase can be resumed after suspend with Addr ("H" or "L") , Data (30h)											
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Temporary Sector Unprotection Mode *2	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Reset from fast Mode *8	2	XXXh	90h	XXXh	00h	—	—	—	—	—	—	—	—
Sector Unlock *9	3	555h	AAh	2AAh	55h	555h	24h	—	—	—	—	—	—
Fast Programming *3	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
Sector Relock *2	2	XXXh	90h	XXXh	F0h or 00h	—	—	—	—	—	—	—	—
Sector Protection Set Function by Extended Sector Protection Command *2	3	555h	AAh	2AAh	55h	555h	24h	—	—	—	—	—	—
Extended sector Protection	3	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—

*1: Either of the two reset commands will reset the device to read mode.

*2: To activate the command, $\overline{OE}$ has to be taken to V_{ID}.

*3: Valid only during Temporary Sector Unprotection mode.

*4: Valid only during Extended Sector Protection Set-up Mode.

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Notes : • Address bits X = “H” or “L” for all address commands except for Program Address (PA) and Sector Address (SA) .

- Bus operations are defined in Table 2.
- RA = Address of the memory location to be read.
  PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ or $\overline{CE}$ pulse.
  SA = Address of the sector to be erased. The combination of A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, and A_{13} will uniquely select any sector.
- RD = Data read from location RA during read operation.
  PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ pulse.
  ID = Device Code. (See Table 4 Autoselect Codes.)
- SPA = Sector Protection Address. Sector Address (SA) and (A_6, A_1, A_0) = (0, 1, 0) to be set.
  SD = Data to verify the Sector Protection. The output at protected Sector = 01h and the output at unprotected Sector = 00h.
- Command combinations not described in “MBM29F004TC/BC Command Definitions Table” are illegal.

Table 4.1 MBM29F004TC/BC Sector Protection Verify Autoselect Codes

Type		A_{18} to A_{13}	A_6	A_1	A_0	Code (HEX)
Manufacture’s Code		X	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	MBM29F004TC	X	V_{IL}	V_{IL}	V_{IH}	77h
	MBM29F004BC	X	V_{IL}	V_{IL}	V_{IH}	7Bh
Sector Protection		Sector Addresses	V_{IL}	V_{IH}	V_{IL}	01h*

* : Outputs 01h at protected sector addresses and outputs 00h at unprotected sector addresses.

Table 4.2 Expanded Autoselect Code Table

Type		Code	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer’s Code		04h	0	0	0	0	0	1	0	0
Device Code	MBM29F004TC	77h	0	1	1	1	0	1	1	1
	MBM29F004BC	7Bh	0	1	1	1	1	0	1	1
Sector Protection		01h	0	0	0	0	0	0	0	1

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 16 K byte, two 8 K bytes, one 32 K byte, and seven 64 K bytes sectors.
- Individual-sector, multiple-sector, or bulk-erase capability.
- Individual or multiple-sector protection is user definable.

Table 5 Sector Address Tables (MBM29F004TC)

Sector Address	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	Address Range
SA0	0	0	0	X	X	X	00000h to 0FFFFh
SA1	0	0	1	X	X	X	10000h to 1FFFFh
SA2	0	1	0	X	X	X	20000h to 2FFFFh
SA3	0	1	1	X	X	X	30000h to 3FFFFh
SA4	1	0	0	X	X	X	40000h to 4FFFFh
SA5	1	0	1	X	X	X	50000h to 5FFFFh
SA6	1	1	0	X	X	X	60000h to 6FFFFh
SA7	1	1	1	0	X	X	70000h to 77FFFh
SA8	1	1	1	1	0	0	78000h to 79FFFh
SA9	1	1	1	1	0	1	7A000h to 7BFFFh
SA10	1	1	1	1	1	X	7C000h to 7FFFFh

Table 6 Sector Address Tables (MBM29F004BC)

Sector Address	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	Address Range
SA0	0	0	0	0	0	X	00000h to 03FFFh
SA1	0	0	0	0	1	0	04000h to 05FFFh
SA2	0	0	0	0	1	1	06000h to 07FFFh
SA3	0	0	0	1	X	X	08000h to 0FFFFh
SA4	0	0	1	X	X	X	10000h to 1FFFFh
SA5	0	1	0	X	X	X	20000h to 2FFFFh
SA6	0	1	1	X	X	X	30000h to 3FFFFh
SA7	1	0	0	X	X	X	40000h to 4FFFFh
SA8	1	0	1	X	X	0	50000h to 5FFFFh
SA9	1	1	0	X	X	1	60000h to 6FFFFh
SA10	1	1	1	X	X	X	70000h to 7FFFFh

Sector	Sector Size	(×8) Address Range
SA0	64 K bytes	00000h to 0FFFFh
SA1	64 K bytes	10000h to 1FFFFh
SA2	64 K bytes	20000h to 2FFFFh
SA3	64 K bytes	30000h to 3FFFFh
SA4	64 K bytes	40000h to 4FFFFh
SA5	64 K bytes	50000h to 5FFFFh
SA6	64 K bytes	60000h to 6FFFFh
SA7	32 K bytes	70000h to 77FFFh
SA8	8 K bytes	78000h to 79FFFh
SA9	8 K bytes	7A000h to 7BFFFh
SA10	16 K bytes	7C000h to 7FFFFh

MBM29F004TC Top Boot Sector Architecture

Sector	Sector Size	(×8) Address Range
SA0	16 K bytes	00000h to 03FFFh
SA1	8 K bytes	04000h to 05FFFh
SA2	8 K bytes	06000h to 07FFFh
SA3	32 K bytes	08000h to 0FFFFh
SA4	64 K bytes	10000h to 1FFFFh
SA5	64 K bytes	20000h to 2FFFFh
SA6	64 K bytes	30000h to 3FFFFh
SA7	64 K bytes	40000h to 4FFFFh
SA8	64 K bytes	50000h to 5FFFFh
SA9	64 K bytes	60000h to 6FFFFh
SA10	64 K bytes	70000h to 7FFFFh

MBM29F004BC Bottom Boot Sector Architecture

■ FUNCTIONAL DESCRIPTION

Read Mode

The MBM29F004TC/BC has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}-t_{OE} time) .

Standby Mode

When using $\overline{CE}$ pin, a CMOS standby mode is achieved with $\overline{CE}$ input held at $V_{CC} \pm 0.3$ V. Under this condition the current consumed is less than 5 μA. A TTL standby mode is achieved with $\overline{CE}$ pin held at V_{IH}. Under this condition the current is reduced to approximately 1 mA. During Embedded Algorithm operation, V_{CC} Active current (I_{CC2}) is required even $\overline{CE} = V_{IH}$. The device can be read with standard access time (t_{CE}) from either of these standby modes. In this mode, all outputs pins are placed in the high impedance state.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}) , output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON'T CARES except A_0, A_1, and A_6. (See Table 4.1 and 4.2.)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29F004TC/BC is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in Table 3. (Refer to Autoselect Command section.)

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer's code (Fujitsu = 04h) and byte 1 ($A_0 = V_{IH}$) represents the device identifier code for MBM29F004TC = 77h, MBM29F004BC = 7Bh. These two bytes are given in the tables 4.1 and 4.2. All identifiers for manufactures and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the Autoselect, A_1 must be V_{IL}. (See Tables 4.1 and 4.2.)

The Autoselect mode also facilitates the determination of sector group protection in the system. By performing a read operation at the address location XX02h with the higher order address bit A_{13}, A_{14}, A_{15}, A_{16}, A_{17} and A_{18} set to the desired sector address, the device will return 01h for a protected sector group and 00h for a non-protected sector.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Group Protection

The MBM29F004TC/BC features hardware sector group protection. These features will disable both program and erase operations in any combination of sectors (0 through 10) . The sector group protection feature is enabled using programming equipment at the user's site. The device is shipped with all sector group unprotected.

To activate command mode sector group protection, the programming groups equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest V_{ID} = 12 V) , $\overline{CE}$ = V_{IL}, A6 = V_{IL}. The sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, and A_{13}) should be set to the sector to be protected. Tables 5 and 6 define the sector address for each of the eleven (11) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See figures 12 and 20 for sector protection waveforms and algorithm.

To verify programming of the command mode sector protection circuitry, the programming equipment must force V_{ID} on address A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, and A_{13}) while (A_6, A_5, A_1, A_0) = (0, 1, 1, 0) will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the device will produce 00h for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, A_5, and A_6 are DON'T CARES. Address locations with A_1 = V_{IL} are reserved for Autoselect manufacturer and device codes.

The alternate hardware sector protect mode intended only for the programming equipment required force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest V_{ID} = 12 V) , $\overline{CE}$ = V_{IL}. The sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, and A_{13}) should be set to the sector to be protected. Tables 4 and 5 define the sector address for each of the eleven (11) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See figures 15 and 23 for sector protection waveforms and algorithm.

To verify programming of the hardware sector protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, and A_{13}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the device will produce 00h for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are DON'T CARES. Address locations with A_1 = V_{IL} are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, and A_{13}) are the desired sector group address will produce a logical "1" at DQ_0 for a protected sector group. See Tables 3.1 and 3.2 for Autoselect codes.

Temporary Sector Unprotection

This feature allows temporary unprotect of previously protected sector of the MBM29F004TC/BC device in order to change data. The Temporary Sector Unprotection mode is activated by setting the $\overline{OE}$ pin to high voltage (12 V) . While $\overline{OE}$ is at V_{ID}, the sector unlock sequence is written to the device. After the sector unlock sequence is written, the $\overline{OE}$ pin is taken back to V_{IH}. The device is now in the Temporary Sector Unprotection mode.

While in this mode, formerly protected sectors can be programmed or erased by selecting the appropriate sector addresses during programming or erase operations. Either sector erase or chip erase operations can be performed in this mode. Exiting the Temporary Sector unprotection mode is accomplished by either removing V_{CC} from the device or by taking $\overline{OE}$ back to V_{ID} and writing the sector relock sequence. After writing the sector relock sequence, the $\overline{OE}$ pin is taken back to V_{IH} and all previously protected sectors will be protected again.

The Temporary Sector Unprotection Status can be used to check whether this mode is in operation or not. The Temporary Sector Unprotection Status can be executed by setting $A_O = A_I = V_{IH}$ ($A_6 = V_{IL}$) during Autoselect mode.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register.

Writing incorrect address and data values or writing them in the improper sequence will reset the device to read mode. Table 3 defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover, both Read/Reset Commands are functionally equivalent, resetting the device to the read mode.

Read/Reset Command

The read or reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory at the Read/Reset operation. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect Command sequence into the command register. Following the command write, a read cycle from address XX00h retrieves the manufacture code of 04h. A read cycle from address XX01h returns the device code (MBM29F004TC = 77h, MBM29F004BC = 7Bh) . (See Tables 4.1 and 4.2)

All manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

Sector state (protect or unprotect) will be informed by address XX02h.

Scanning the sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, and A_{13}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical “1” at device output DQ_0 for a protected sector group.

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register and also to write the Autoselect command during the operation, execute it after writing Read/Reset command sequence.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the device returns to the read mode and addresses are no longer latched. (See Table 6, Hardware Sequence Flags.) Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

If a hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Reset/Read mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

Figure 16 illustrates the Embedded Programming™ Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ_7 is “1” (See Write Operation Status section) at which time the device returns to read the mode.

Figure 17 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) , while the command (Data = 30h) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) . After time-out of 50 μs from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command (30h) to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50 μs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50 μs from the rising edge of the last $\overline{CE}$ or $\overline{WE}$ will initiate the execution of the Sector Erase command (s) . If another falling edge of the $\overline{CE}$ or $\overline{WE}$ occurs within the 50 μs time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, Write Operation Status section for DQ_3, Sector Erase Timer operation.) Resetting the device once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 6) .

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector (s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 50 μs time out from the rising edge of the $\overline{CE}$ or $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ_7 is “1” (See Write Operation Status section) at which time the device returns to the read mode. $\overline{Data}$ polling must be performed at an address within any of the sectors being erased.

Figure 17 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable only during a Sector Erase operation which includes the time-out period for sector erase and will be ignored during Chip Erase or Programming

operations. Writing the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Any other command written during the Erase Suspend mode will be ignored except the Erase Resume command. Writing the Erase Resume command resumes the erase operation. The addresses are “DON’T CARES” when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 15 μs to suspend the erase operation. When the device has entered the erase-suspended mode, the DQ_7 bit will be at logic “1” and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Byte Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended program operation is detected by the $\overline{\text{Data}}$ polling of DQ_7, or by the Toggle Bit I (DQ_6) which is the same as the regular Byte Program operation. Note that DQ_7 must be read from the Byte Program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Extended Command

(1) Fast Mode

MBM29F004TC/BC has Fast Mode function. This feature allows the system to program the device faster than using the standard program command sequence. The fast mode command sequence is initiated by setting the $\overline{\text{OE}}$ pin to V_{ID} and writing two unlock cycles. This is followed by a third write cycle containing the fast mode command, 20h. The device then enters the fast mode. Previously protected sectors of the device are now temporarily unprotected. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standerd program command sequence, resulting in faster total programming time. Tables 6 and 7 show the requirements for the command sequence.

During the unlock bypass mode, only the Fast Program and Reset from Fast Mode commands are valid. To exit the fast mode, the system must issue the two-cycle unlock bypass reset command sequence with $\overline{\text{OE}}$ at V_{ID}. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don’t care for both cycles. The device then returns to reading array data. (Refer to the Figure 24 Extended algorithm.)

(2) Fast Programming

During Temporary Sector Unprotection Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD) .

Sector Relock

To relock Temporary Sector Unprotection or Extended Sector Protection, $\overline{\text{OE}}$ pin should be forced to V_{2H} after Relock Sector command sequence with OE pin, that is forced V_{ID}.

Extended Sector Protection Set-up

This function operation is for the execution of Extended Sector Protection. This mode is excuted by forcing V_{IH} on $\overline{OE}$ pin after a command sequences with $\overline{OE}$ pin, that is forced V_{ID}.

Extended Sector Protection/Extended Sector Protection Set-up

In this mode, the operation is initiated by writing the set-up command (60h) into the command register after Extended Sector Protection Set-up command. Then, the sector addresses pin (A_6, A_1, A_0) = (0, 1, 0) should be set to the sector to be protected (recommend to set V_{IL} for the other addresses pins) , and write Extended Sector Protection Command (60h) . A sector is typically protected in 100 µs. To verify programming of the protection circuitry, the sector addresses pins (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40h) . Following the command write, a logical "1" at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical "0", please repeat to write Extended Sector Protection command (60h) again. To terminate the operation it is necessary relock the sector.
This command is the same function as the Sector Protection.

Write Operation Status

Detailed in Table 8 are all the status flags that can be used to check the status of the device for current mode operation. During sector erase, the part provides the status flags automatically to the I/O ports. The information on DQ_2 is address sensitive. This means that if an address from an erasing sector is consecutively read, then the DQ_2 bit will toggle. However, DQ_2 will not toggle if an address from a non-erasing sector is consecutively read. This allows the user to determine which sectors are erasing and which are not.

Once erase suspend is entered, address sensitivity still applies. If the address of a non-erasing sector (that is, one available for read) is provided, then stored data can be read from the device. If the address of an erasing sector (that is, one unavailable for read) is applied, the device will output its status bits.

Table 6 Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle*1	0	0	1*2
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

*1 : Performing successive read operations from any address will cause DQ_6 to toggle.

*2 : Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the DQ_2 bit. However, successive reads from the erase-suspended sector will cause DQ_2 to toggle.

Notes : • DQ_0 and DQ_1 are reserve pins for future use.
• DQ_4 is Fujitsu internal use only.

DQ_7
Data Polling

The MBM29F004TC/BC device features Data Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ_7. The Data polling is valid after the rising edge of the forth write pulse sequence. During the Embedded Erase™ Algorithm, an attempt to read the device will produce a "0" at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ_7 output. The flowchart for Data Polling (DQ_7) is shown in Figure 18.

Data Polling will also flag the entry into Erase Suspend. DQ_7 will switch "0" to "1" at the start of the Erase Suspend mode. Please note that the address of an erasing sector must be applied in order to observe DQ_7 in the Erase Suspend Mode.

During Program in Erase Suspend, Data Polling will perform the same as in regular program execution outside of the suspend mode.

For Chip Erase and Sector Erase, the Data Polling is valid after the rising edge of the sixth WE pluse in the six write pulse sequence. Data Polling must be performed at sector address within any of the sectors being programmed or erased. Otherwise, the status may not be valid and Data Polling at a protected sector may not be correctly performed. In this case, the Toggle Bit I will be recommended.

Just prior to the completion of Embedded Algorithm operation, MBM29F004TC/BC data pins (DQ_7) may change asynchronously while the output enable (OE) is asserted low. This means that the device is driving status information on DQ_7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ_7 has a valid data, the data outputs on DQ_0 to DQ_6 may be still invalid. The valid data on DQ_0 to DQ_7 will be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspend, or sector erase time-out.

See Figure 9 for the Data Polling timing specifications and waveforms.

DQ_6
Toggle Bit I

The MBM29F004TC/TB also features the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (OE toggling) data from the device will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth WE pulse in the four write pulse sequence. For Chip Erase and Sector Erase, the Toggle Bit I is valid after the rising edge of the sixth WE pulse in the six write pulse sequence. The Toggle Bit I is active during the Sector Erase time out.

In programming, if the sector being written to is protected, the Toggle Bit I will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the Toggle Bit I for about 100 µs and then drop back into read mode, having changed none of the data.

Either CE or OE toggling will cause the DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ_6 to toggle.

See Figure 10 for the Toggle Bit I timing specifications and diagrams.

DQ_5
Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count) . Under these conditions DQ_5 will produce a “1”. This is a failure condition which indicaters that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling DQ_7, DQ_6 is only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA) . The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 2.
The DQ_5 failure condition may also appear if a user tries to program a 1 to a location that is previously programmed to 0. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ_7 bit and DQ_6 never stops toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a “1”. Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device with command sequence.

DQ_3
Sector Erase Timer

After the completion of the initial Sector Erase command sequence, the Sector Erase time-out will begin. DQ_3 will remain low until the time-out is completed. $\overline{\text{Data}}$ Polling and Toggle Bit I are valid after the initial Sector Erase command sequence.
If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ_3 may be used to determine if the Sector Erase timer window is still open. If DQ_3 is high (“1”) , the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit I. If DQ_3 is low (“0”) the device will accept additional Sector Erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.
Refer to Table 6 : Hardware Sequence Flags.

DQ_2
Toggle Bit II

This Toggle Bit II, along with DQ_6, can be used to determine whether the device is in the Embedded Erase™ Algorithm or in Erase Suspend.
Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase™ Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic “1” at the DQ_2 bit.
DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress.
For example, DQ_2 and DQ_6 can be used together to determine the erase-suspend-read mode (DQ_2 toggles while DQ_6 does not) . See also Table 6 and Figure 14.
Furthermore, DQ_2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ_2 toggles if this bit is read from the erasing sector.

Table 9 Toggle Bit Status

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggles	1
Erase	0	Toggles	Toggles
Erase-Suspend Read*1 (Erase-Suspended Sector)	1	1	Toggles
Erase-Suspend Program	$\overline{DQ_7}$*2	Toggles	1*2

*1 : These status flags apply when outputs are read from a sector that has been erase-suspended.
*2 : These status flags apply when outputs are read from the byte address of the non-erase suspended sector.

Data Protection

The MBM29F004TC/BC is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completions of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V) . If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

The Embedded Program Algorithm will be stopped under the V_{CC} level is less than V_{LKO}. The Embedded Program Algorithm will not be restart even if the V_{CC} level satisfy the recommended V_{CC} supply voltage again.

Then, if the Embedded Program Algorithm is stopped during the program ro erase operation is in progress, the address data is not correct and the programming or erase command should be written again.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Unprotection

MBM29F004TC/BC features hardware Sector Protection at user’s side. This feature will disable both program and erase operations in protected sectors. The programming and erase command to the protected sector will be ignored.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	−55	+125	°C
Ambient Temperature with Power Applied	T_A	−40	+85	°C
Voltage with Respect to Ground All Pins except A_9 and $\overline{OE}$*1, *2	V_{IN}, V_{OUT}	−2.0	+7.0	V
V_{CC}*1, *2	V_{CC}	−2.0	+7.0	V
A_9 and $\overline{OE}$*1, *3	V_{IN}	−2.0	+13.5	V

*1 : Voltage : GND = 0 V

*2 : Minimum DC voltage on input and I/O pins are −0.5 V. During voltage transitions, inputs may undershoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins are V_{CC} + 0.5 V. During voltage transitions, inputs may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

*3 : Minimum DC input voltage on A_9 and $\overline{OE}$ pins are −0.5 V. During voltage transitions, A_9, $\overline{OE}$ pins are + 13.0 V which may overshoot to 14.0 V for periods of up to 20 ns. Voltage difference between input voltage and power supply.
(V_{IN} − V_{CC}) do not exceed 9 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Parameter	Symbol	Part No.	Value			Unit
			Min	Typ	Max	
Ambient Temperature	T_A	MBM29F004TC/BC-70	−20	—	+70	°C
		MBM29F004TC/BC-90	−40	—	+85	°C
V_{CC} Supply Voltage	V_{CC}	MBM29F004TC/BC-70/-90	+4.5	5.0	+5.5	V
	GND			0		

Note : Operating ranges define those limits between which the proper device function is quaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT

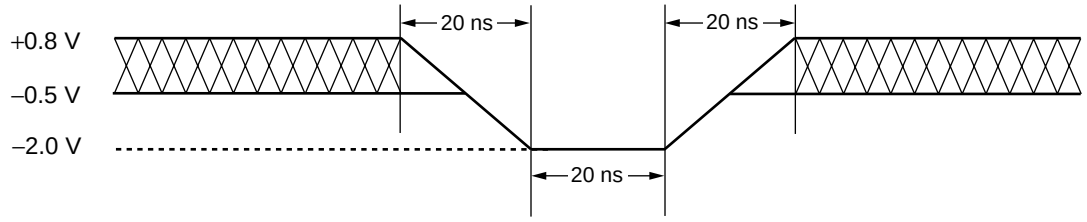


Figure 1 Maximum Undershoot Waveform

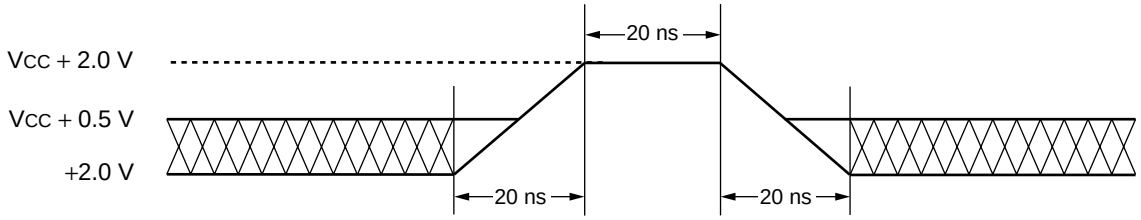
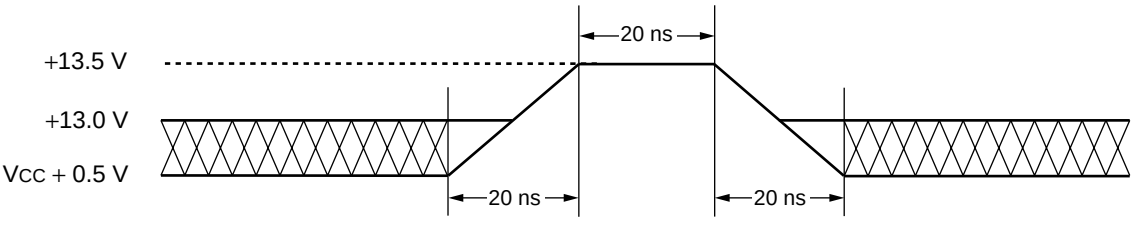


Figure 2 Maximum Overshoot Waveform 1



Note : This waveform is applied for A_9 and $\overline{OE}$.

Figure 3 Maximum Overshoot Waveform 2

■ DC CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max	−1.0	—	+ 1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max	−1.0	—	+ 1.0	µA
A_9, $\overline{OE}$ Inputs Leakage Current	I_{LIT}	V_{CC} = V_{CC} Max, A_9, $\overline{OE}$ = 12.5 V	—	—	+ 50	µA
V_{CC} Active Current*1	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	—	—	35	mA
V_{CC} Active Current*2	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	—	—	50	mA
V_{CC} Current (Standby)	I_{CC3}	V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{IH}	—	—	1	mA
		V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{CC} ± 0.3 V	—	1	5	µA
Input Low Level	V_{IL}	—	−0.5	—	0.8	V
Input High Level	V_{IH}	—	2.0	—	V_{CC} + 0.5	V
Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$) *3, *4	V_{ID}	—	11.5	12	12.5	V
Output Low Voltage Level	V_{OL}	I_{OL} = 5.8 mA, V_{CC} = V_{CC} Min	—	—	0.45	V
Output High Voltage Level	V_{OH1}	I_{OH} = −2.5 mA, V_{CC} = V_{CC} Min	2.4	—	—	V
	V_{OH2}	I_{OH} = −100 µA	V_{CC} − 0.4	—	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—	3.2	3.7	4.2	V

*1 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz) .
The frequency component typically is 2 mA/MHz, with $\overline{OE}$ at V_{IH}.

*2 : I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3 : Applicable to sector protection function.

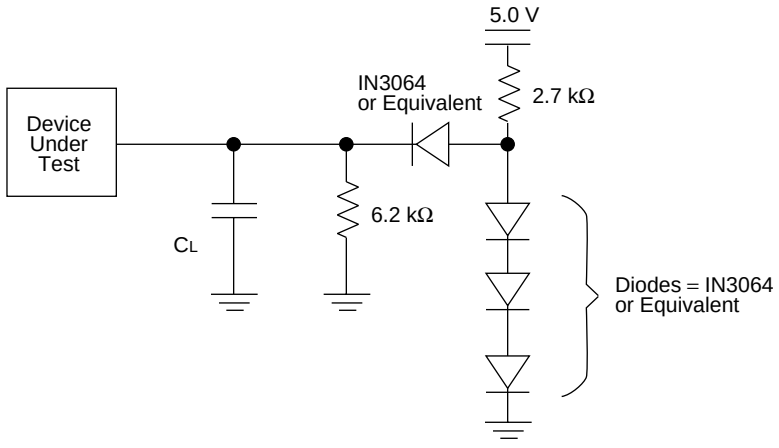
*4 : (V_{ID} − V_{CC}) do not exceed 9.0 V.

■ AC CHARACTERISTICS

- **Read Only Operations Characteristics**

Parameter	Symbol		Test Setup	Value (Note)				Unit
				-70		-90		
	JEDEC	Standard		Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	70	—	90	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	70	—	90	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	70	—	90	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	30	—	35	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	20	—	20	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	20	—	20	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	0	—	ns

Note : Test Conditions :
Output Load : 1 TTL gate and 100 pF
Input rise and fall times : 5 ns
Input pulse levels : 0.45 V or 2.4 V
Timing measurement reference level
Input : 0.8 V and 2.0 V
Output : 0.8 V and 2.0 V



Note : C_L = 100 pF including jig capacitance

Figure 4 Test Conditions

- **Write/Erase/Program Operations**

Parameter		Symbol		Value (Note)						Unit
				-70			-90			
		JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
Write Cycle Time		t_{AVAV}	t_{WC}	70	—	—	90	—	—	ns
Address Setup Time		t_{AVWL}	t_{AS}	0	—	—	0	—	—	ns
Address Hold Time		t_{WLAX}	t_{AH}	45	—	—	45	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	30	—	—	45	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	0	—	—	ns
Output Enable Setup Time		—	t_{OES}	0	—	—	0	—	—	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	—	0	—	—	ns
	Toggle Bit I and $\overline{\text{Data}}$ Polling			10	—	—	10	—	—	ns
Read Recover Time before Write		t_{GHWL}	t_{GHWL}	0	—	—	0	—	—	ns
Read Recover Time before Write		t_{GHEL}	t_{GHEL}	0	—	—	0	—	—	ns
$\overline{\text{CE}}$ Setup Time		t_{ELWL}	t_{CS}	0	—	—	0	—	—	ns
$\overline{\text{WE}}$ Setup Time		t_{WLEL}	t_{WS}	0	—	—	0	—	—	ns
$\overline{\text{CE}}$ Hold Time		t_{WHEH}	t_{CH}	0	—	—	0	—	—	ns
$\overline{\text{WE}}$ Hold Time		t_{EHWH}	t_{WH}	0	—	—	0	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	35	—	—	45	—	—	ns
$\overline{\text{CE}}$ Pulse Width		t_{ELEH}	t_{CP}	35	—	—	45	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	20	—	—	20	—	—	ns
$\overline{\text{CE}}$ Pulse Width High		t_{EHEL}	t_{CPH}	20	—	—	20	—	—	ns
Byte Programming Operation		t_{WHWH1}	t_{WHWH1}	—	8	—	—	8	—	µs
Sector Erase Operation *1		t_{WHWH2}	t_{WHWH2}	—	1	—	—	1	—	s
				—	—	8	—	—	8	s
V_{CC} Setup Time		—	t_{VCS}	50	—	—	50	—	—	µs
Voltage Transition Time *2		—	t_{VLHT}	4	—	—	4	—	—	µs
Write Pulse Width *2		—	t_{WPP}	100	—	—	100	—	—	µs
$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active *2		—	t_{OESP}	4	—	—	4	—	—	µs
$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active *2		—	t_{CSP}	4	—	—	4	—	—	µs
V_{ID} Rise and Fall Time		—	t_{VIDR}	500	—	—	500	—	—	ns
Delay Time from Embedded Output Enable		—	t_{EOE}	30	—	—	35	—	—	ns

*1: This does not include the preprogramming time.

*2: This timing is only for Sector Protection operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	1	8	s	Excludes programming time prior to erasure
Byte Programming Time	—	8	150	µs	Excludes system-level overhead
Chip Programming Time	—	4.2	10	s	Excludes system-level overhead
Program/Erase Cycle	100,000	—	—	cycle	—

■ PIN CAPACITANCE

1.TSOP (1)

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	7	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	8	10	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	8.5	10	pF

Note : Test conditions T_A = 25 °C, f = 1.0 MHz

2.QFJ

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	7	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	8	10	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	8.5	10	pF

Note : Test conditions T_A = 25 °C, f = 1.0 MHz

■ TIMING DIAGRAM

- **Key to Switching Waveforms**

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Change from H to L
	May Change from L to H	Will Be Change from L to H
	"H" or "L": Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

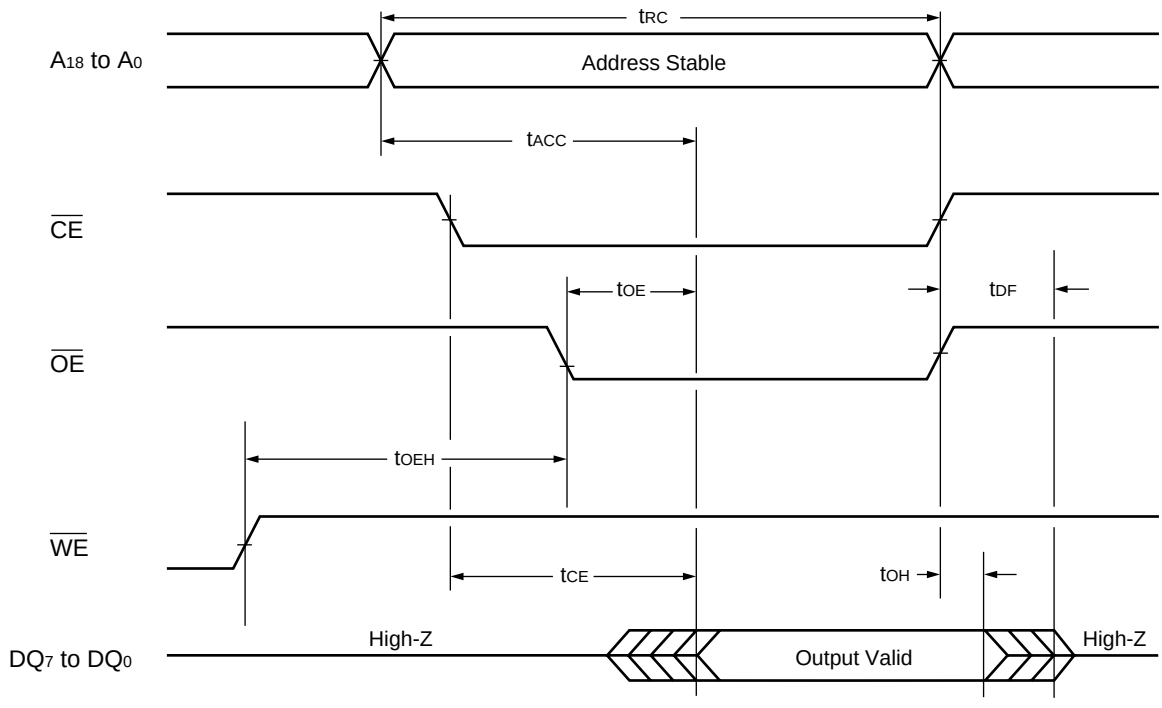


Figure 5.1 AC Waveforms for Read Operation

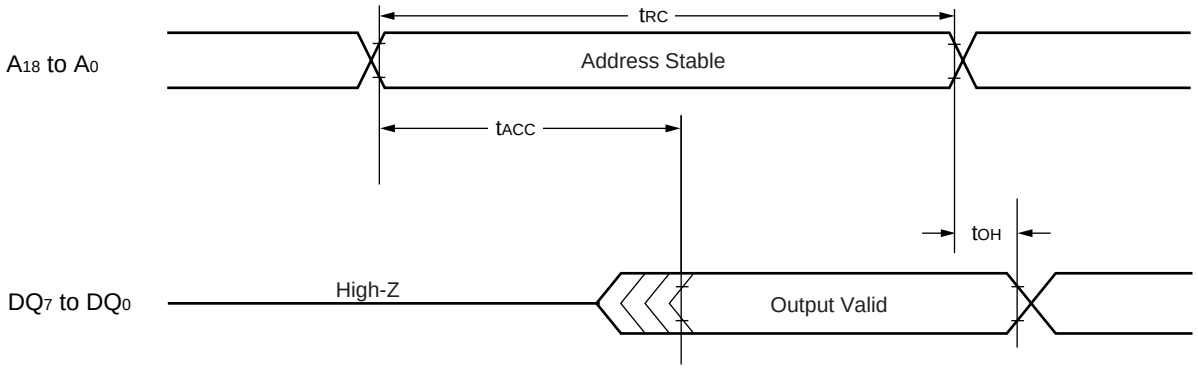
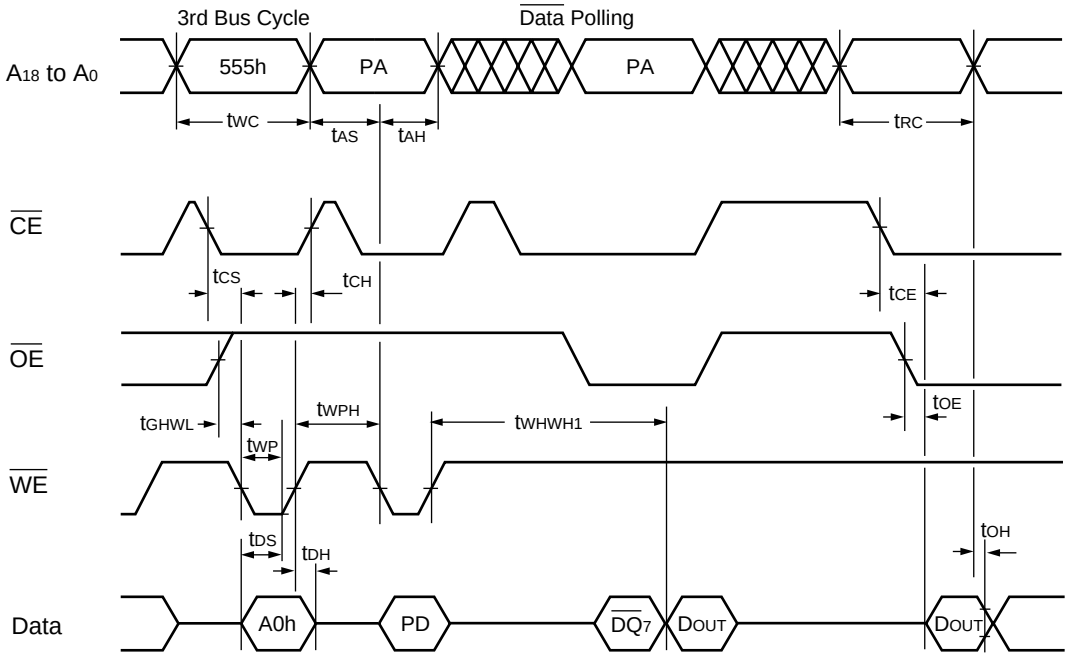
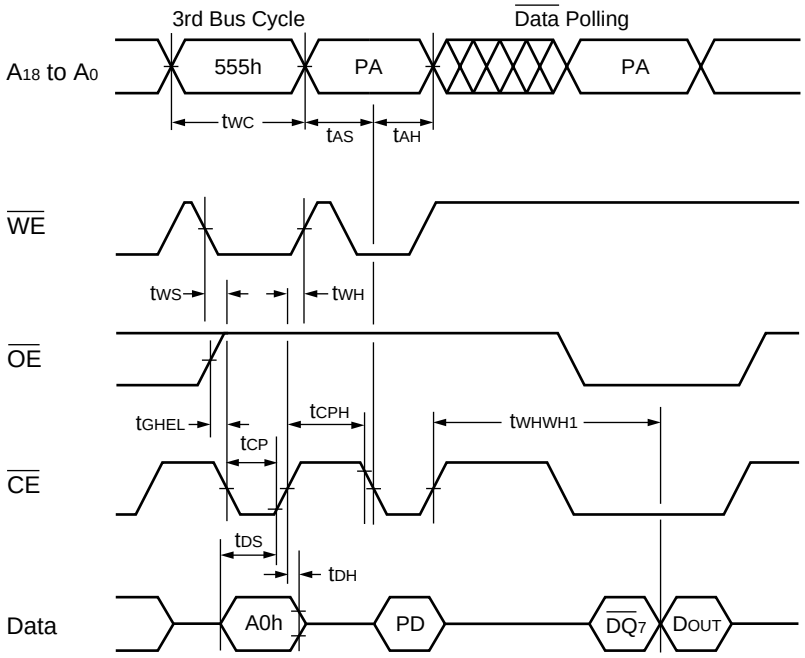


Figure 5.2 AC Waveforms for Read Operation



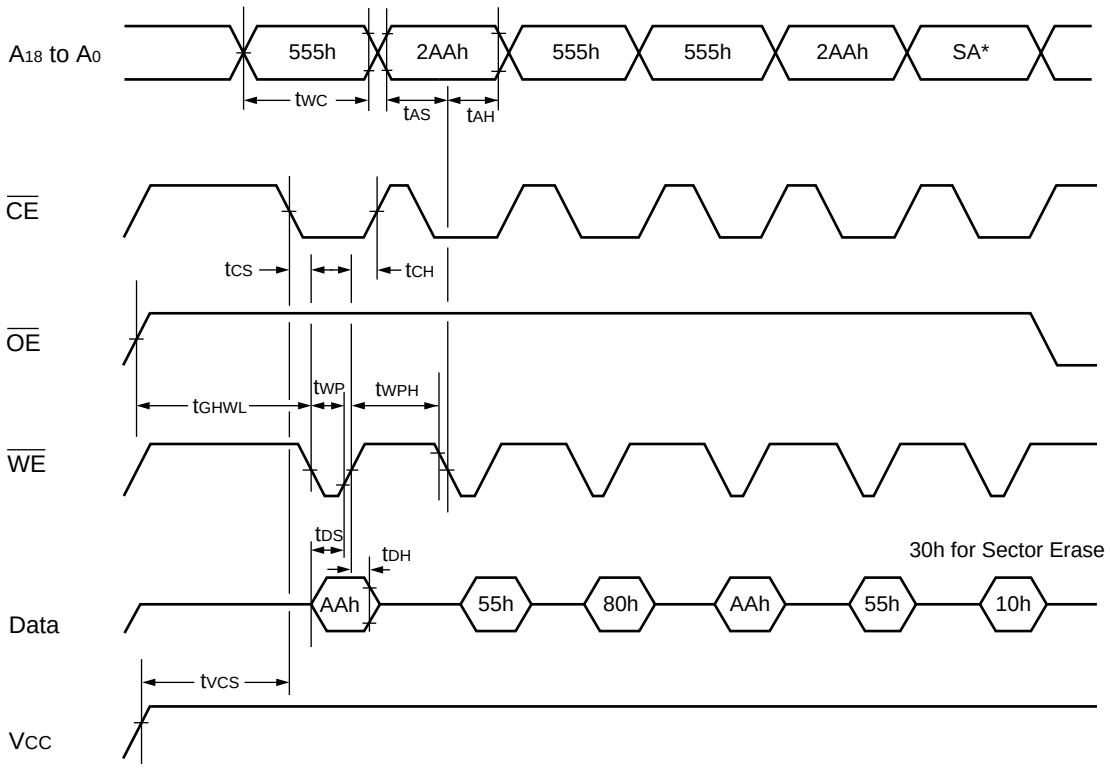
Notes : • PA is address of the memory location to be programmed.
- PD is data to be programmed at word address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.

Figure 6 AC Waveforms for Alternate $\overline{WE}$ Controlled Program Operation



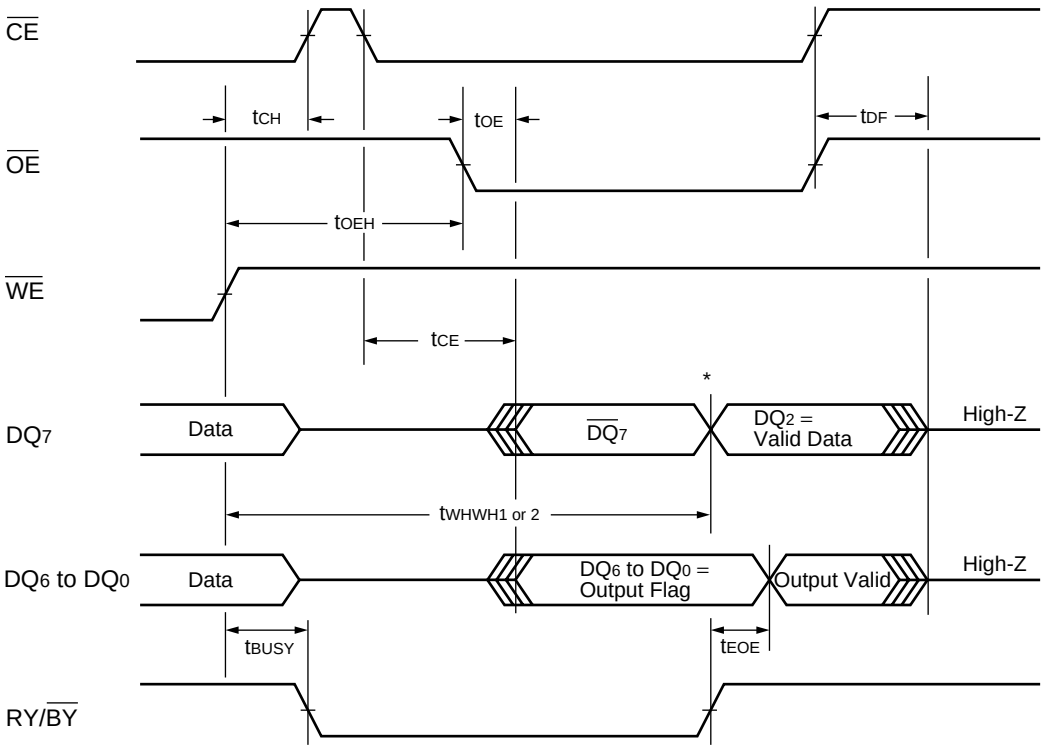
Notes : • PA is address of the memory location to be programmed.
- PD is data to be programmed at word address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- This command requires Sector Protection Set-up.

Figure 7 AC Waveforms for Alternate $\overline{CE}$ Controlled Program Operation



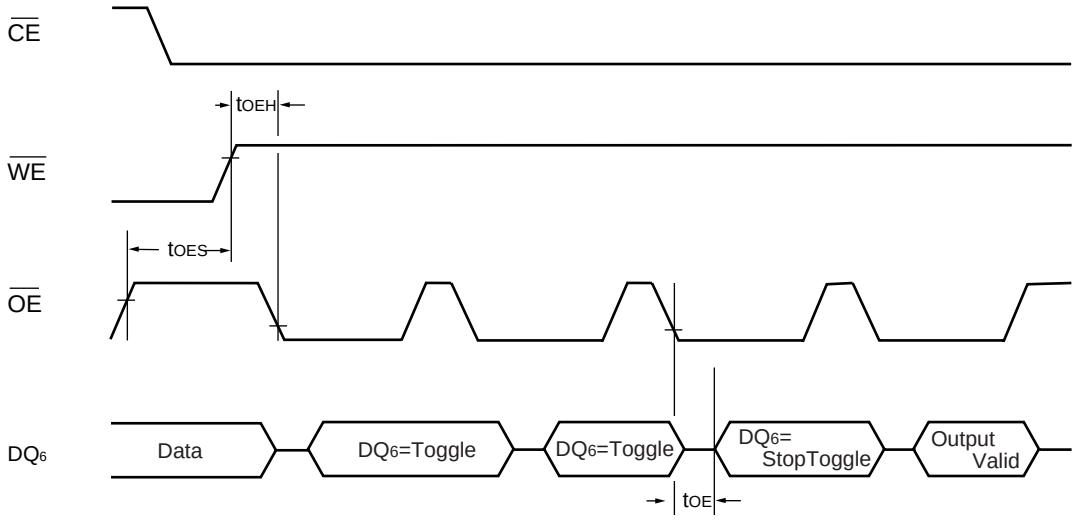
* : SA is the sector address for Sector Erase. Addresses = 555h (Word) for Chip Erase.

Figure 8 AC Waveforms for Chip/Sector Erase Operation



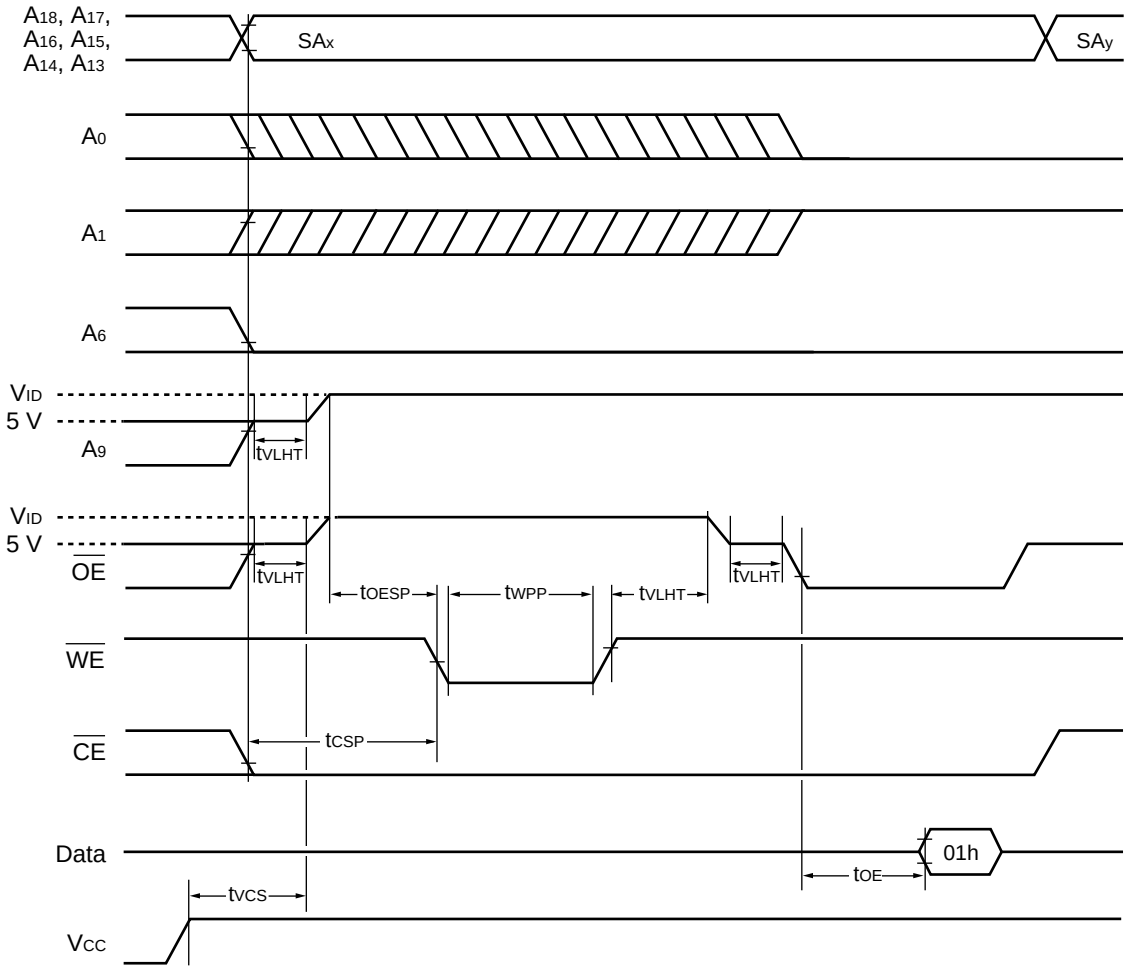
* : DQ_7 = Valid Data (The device has completed the Embedded operation) .

Figure 9 AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operation



Note : DQ_6 : Stop toggling (The device completes the automatic operation.)

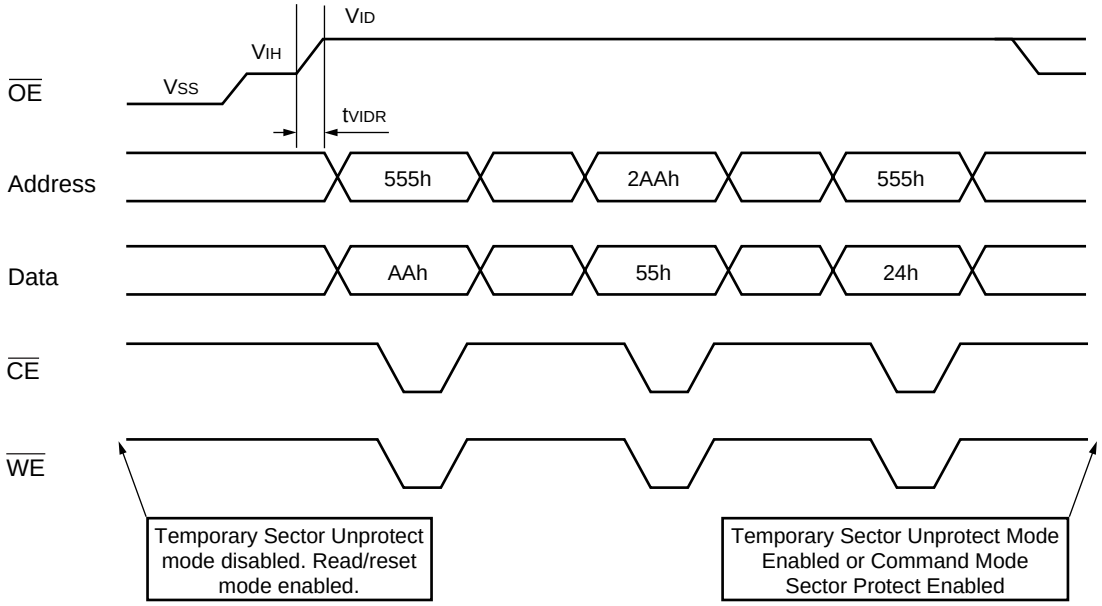
Figure 10 AC Waveforms for Toggle Bit



SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected

Note : A_{-1} is V_{IL} on byte mode.

Figure 11 AC Waveforms Sector Protection



Notes : • To enable Temporary Sector Unprotection Mode, write 20h in data; to enable Command Mode Sector Protect, write 24h in data.
• To enable Temporary Sector Unprotection Mode, $\overline{OE}$ must be at V_{IH}; to enter Command Mode Sector Protect, $\overline{OE}$ must be held at V_{ID}.

Figure 11 3-Byte Sector Unlock Sequence Timing Diagram

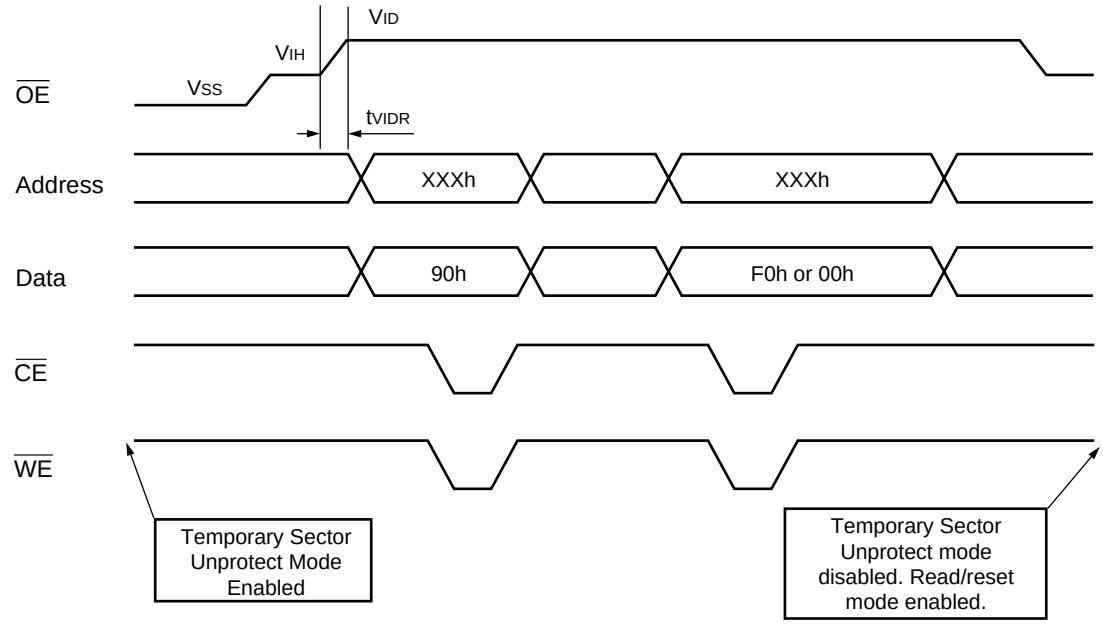
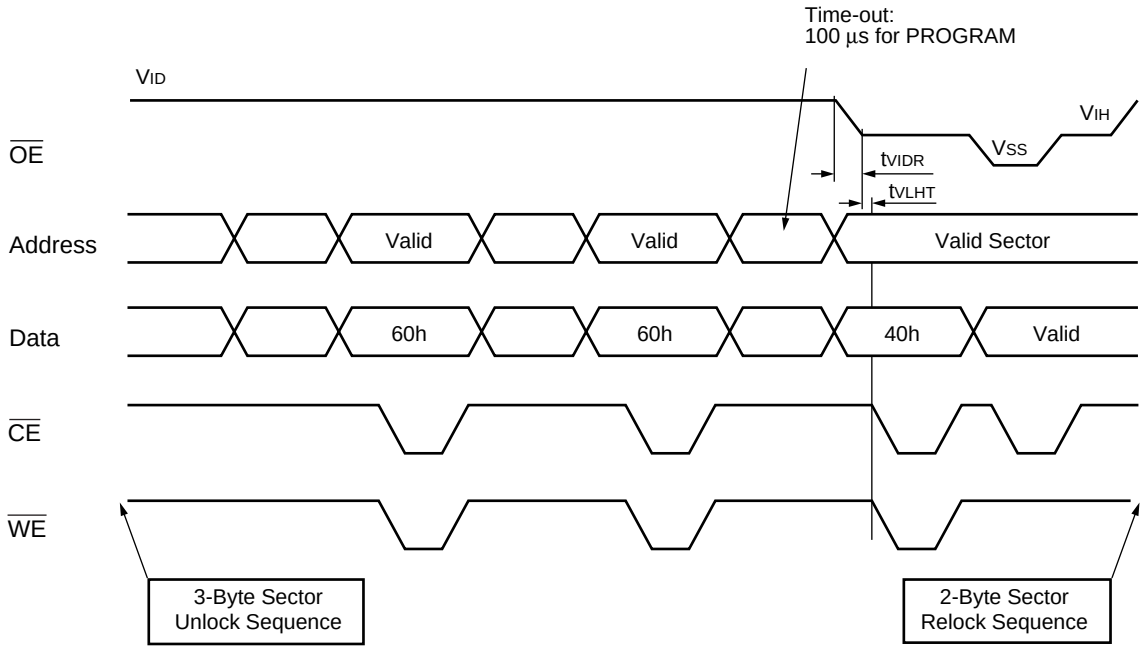
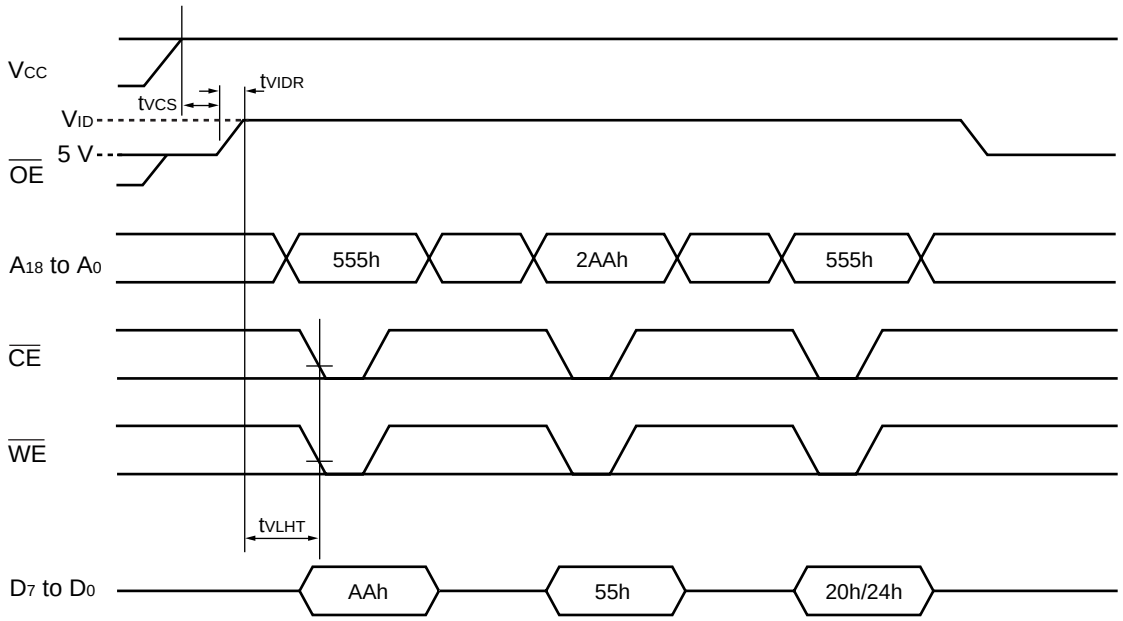


Figure 12 2-Byte Sector Relock Sequence Timing Diagram



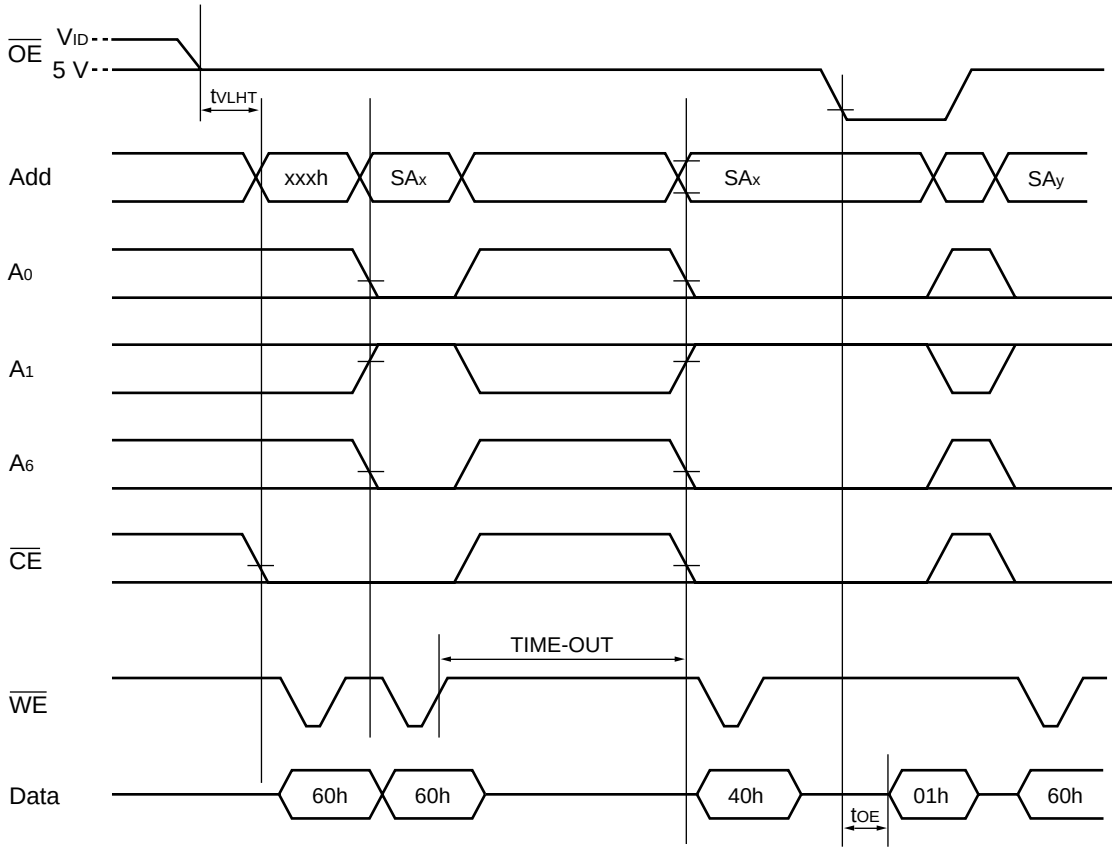
Notes : • To enable the Command Mode Sector Protect, write 24h in data in 3-Byte Unlock Sequence.
• For sector protect, $A_6 = 0$, $A_5 = 1$, $A_1 = 1$, $A_0 = 0$.

Figure 13 AC Waveforms for Command Mode Sector Protect Timing Diagram



Note : To execute Temporary Sector Unprotection mode, 20h should be written.
To execute Extended Sector Protection mode, 24h should be written.

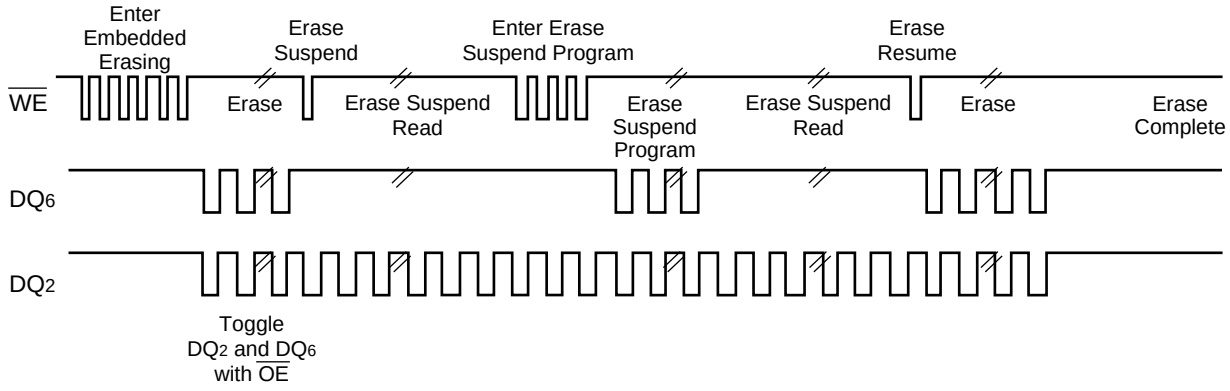
Figure 12 AC Waveforms for Temporary Sector Unprotection/Extended Sector-Protection set-up



SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
TIME-OUT : Time-Out Window = 100 µs (Min)

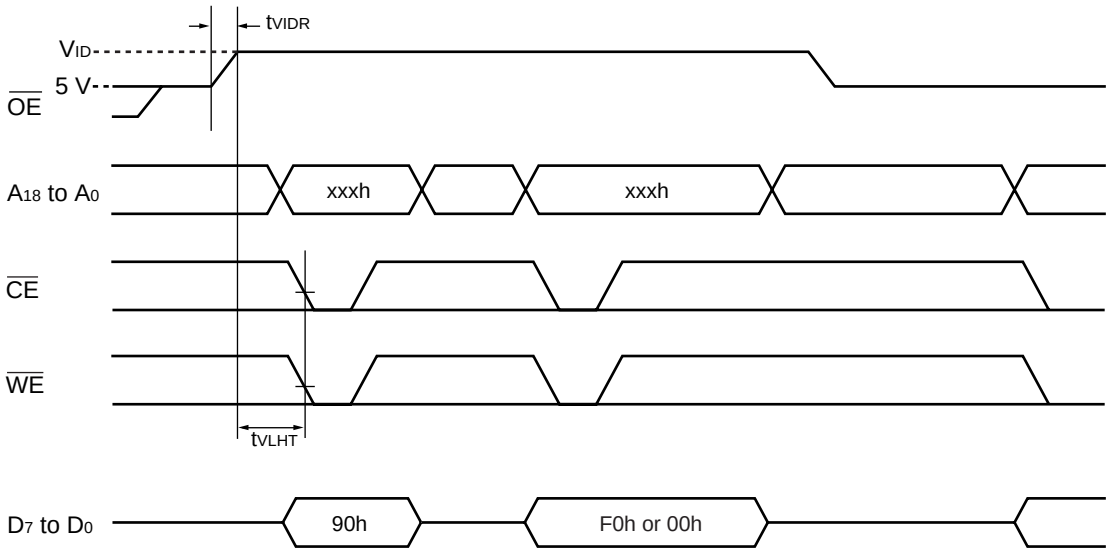
Note : This command requires Sector Protection Set-up

Figure 13 AC Waveforms for Extended Sector Protection



Note : DQ_2 is read from the erase-suspended sector.

Figure 14 DQ_2 vs. DQ_6



Note : This command is to complete Temporary Sector Unprotection mode or Extended Sector Protection.

Figure 15 AC Waveforms for Sector Relock

■ FLOW CHART

EMBEDDED ALGORITHM

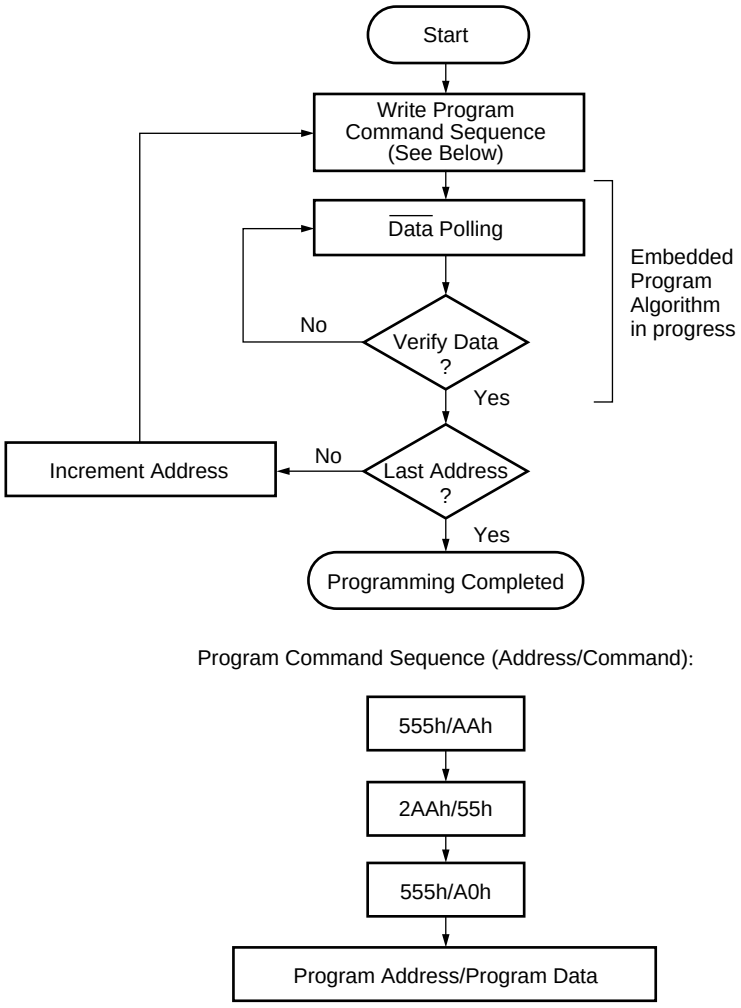


Figure 16 Embedded Program™ Algorithm

EMBEDDED ALGORITHM

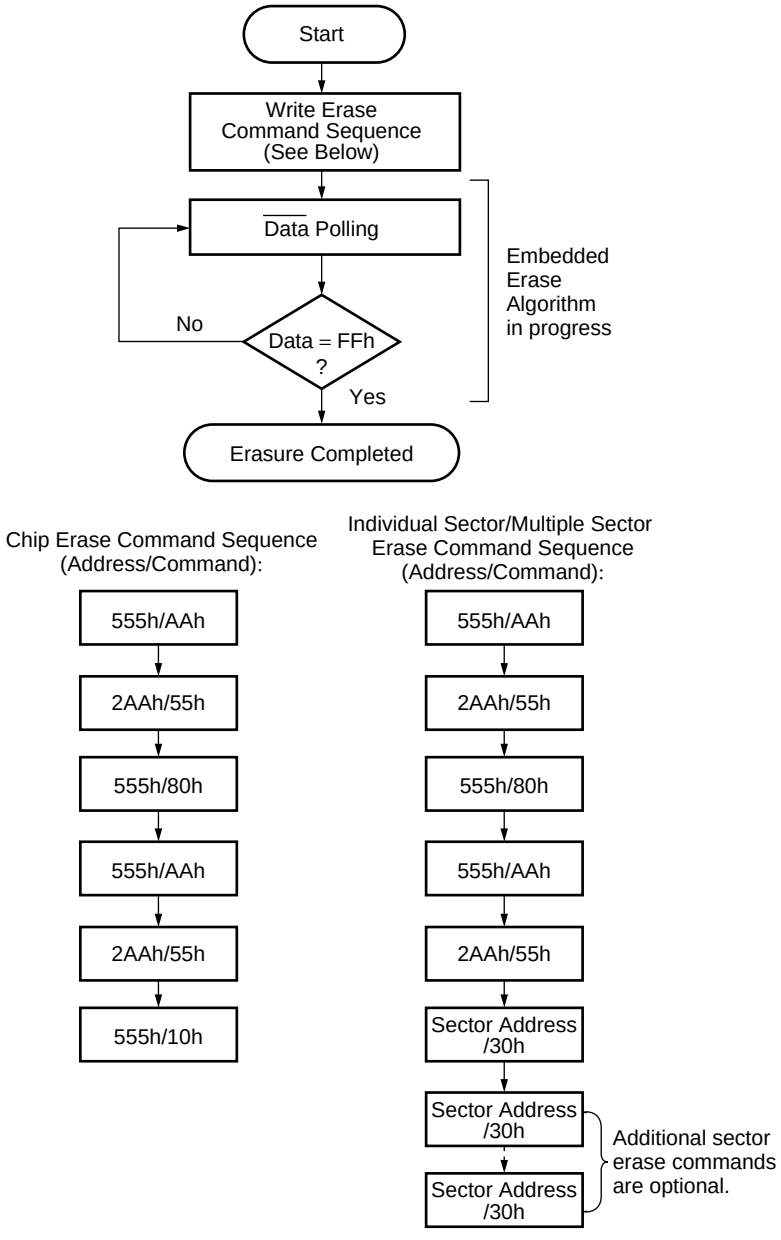
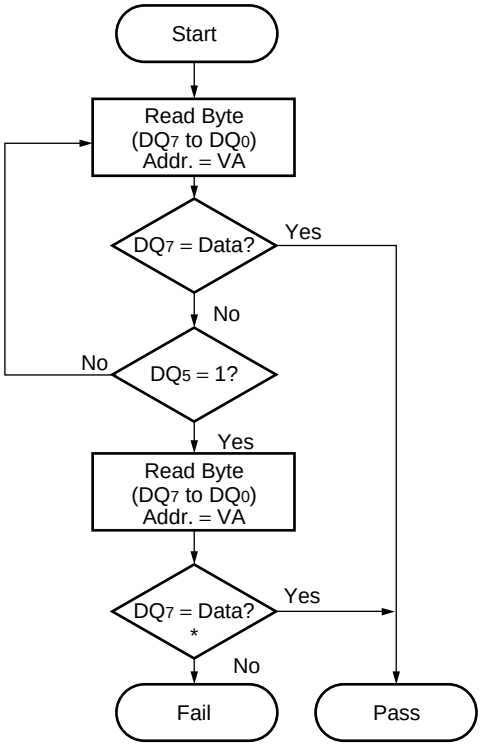


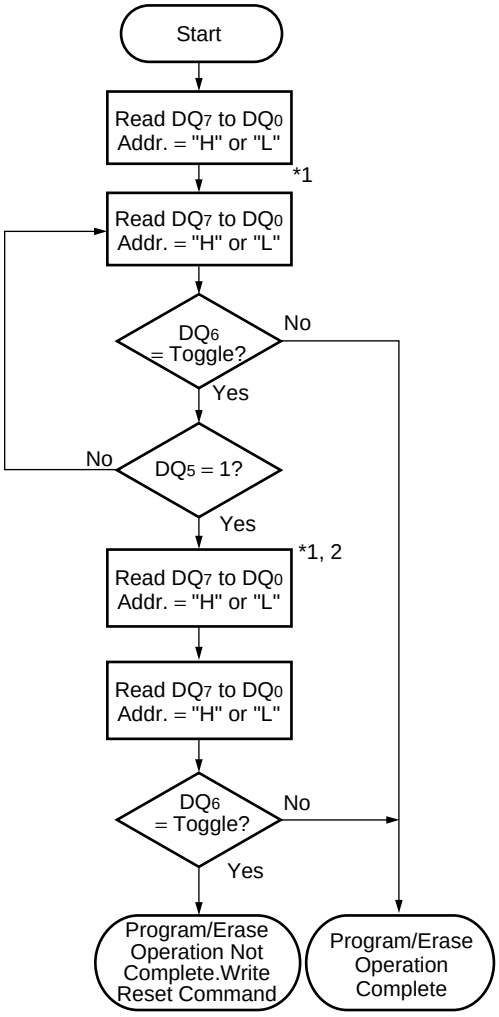
Figure 17 Embedded Erase™ Algorithm



* : DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.

Note: VA = Address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple erases operation.
= Any of the sector group addresses within the sector not being protected during sector erase or multiple sector erases operation.

Figure 18 $\overline{\text{Data}}$ Polling Algorithm



*1 : Read toggle bit twice to determine whether it is toggling.

*2 : Recheck toggle bit because it may stop toggling as DQ_5 changes to “1”.

Figure 19 Toggle Bit Algorithm

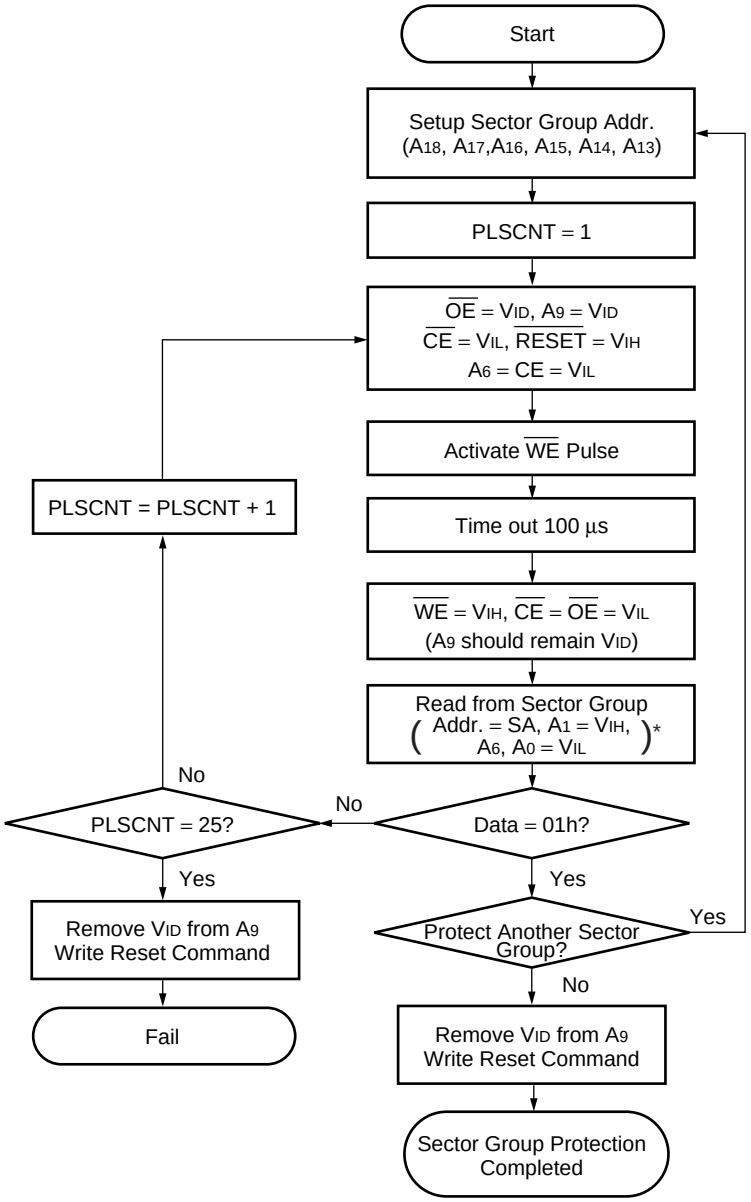
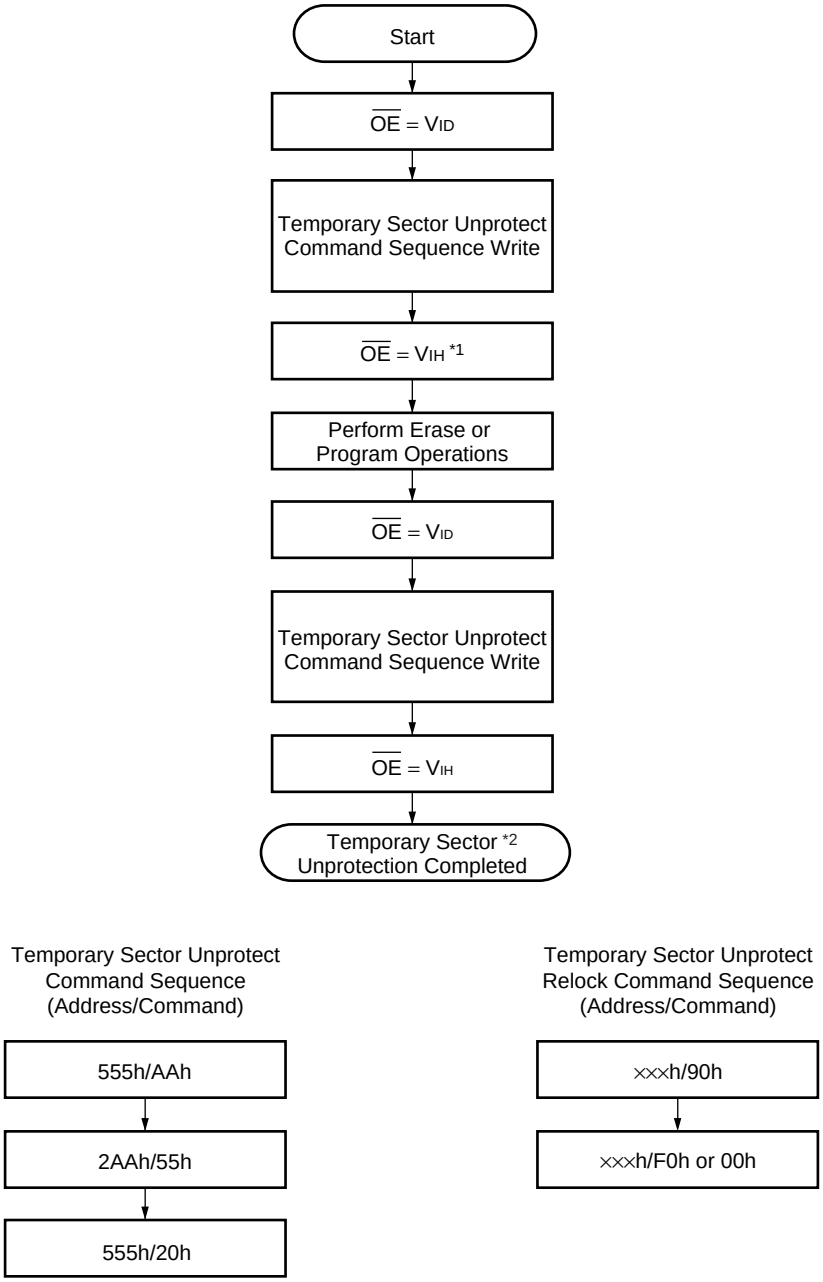


Figure 20 Sector Group Protection Algorithm



*1 : All protected sectors are unprotected.

*2 : All previously protected sectors are protected once again.

Figure 21 Temporary Sector Unprotection Algorithm

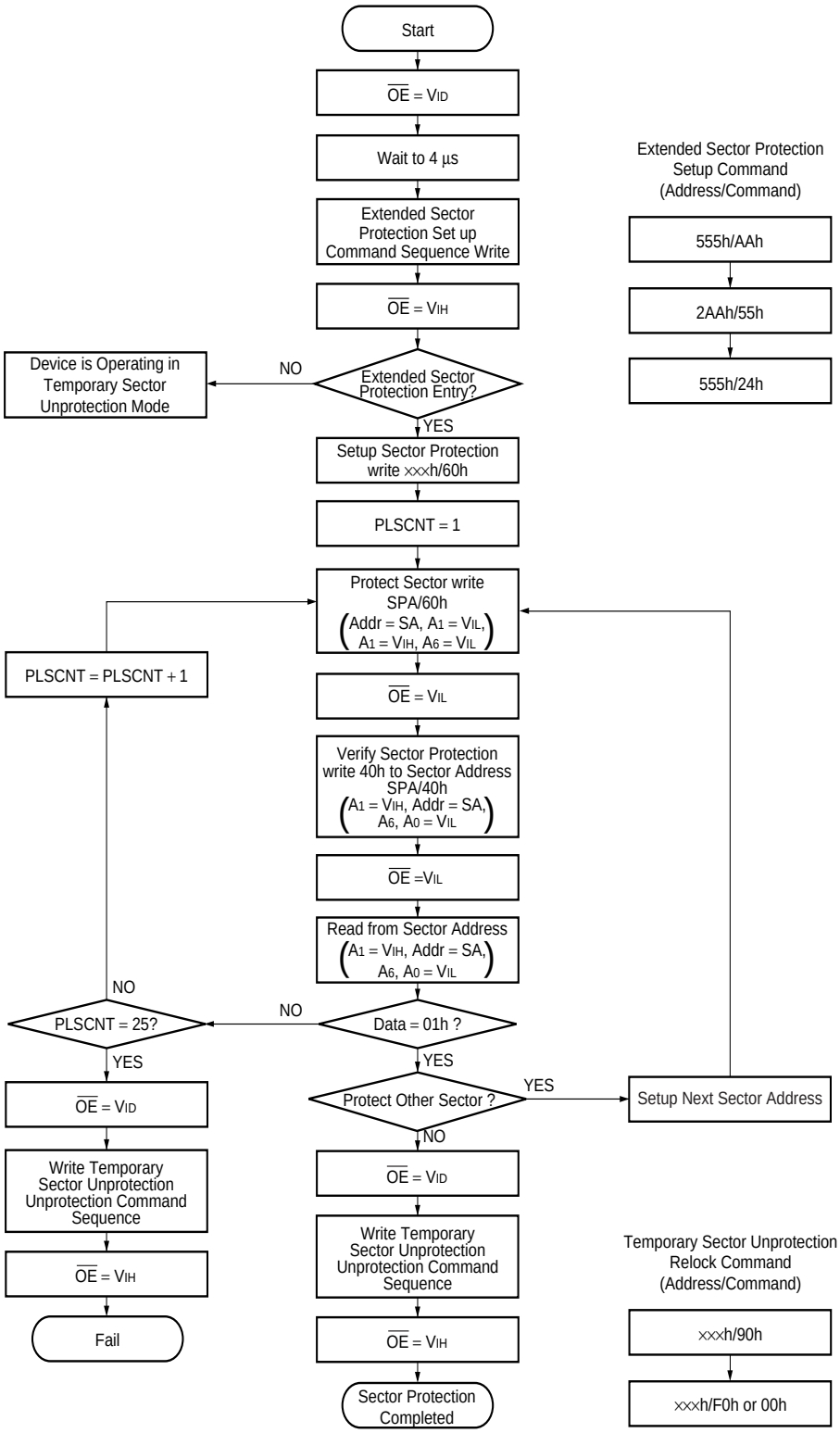


Figure 22 Extended Sector Protection Algorithm

FAST MODE ALGORITHM

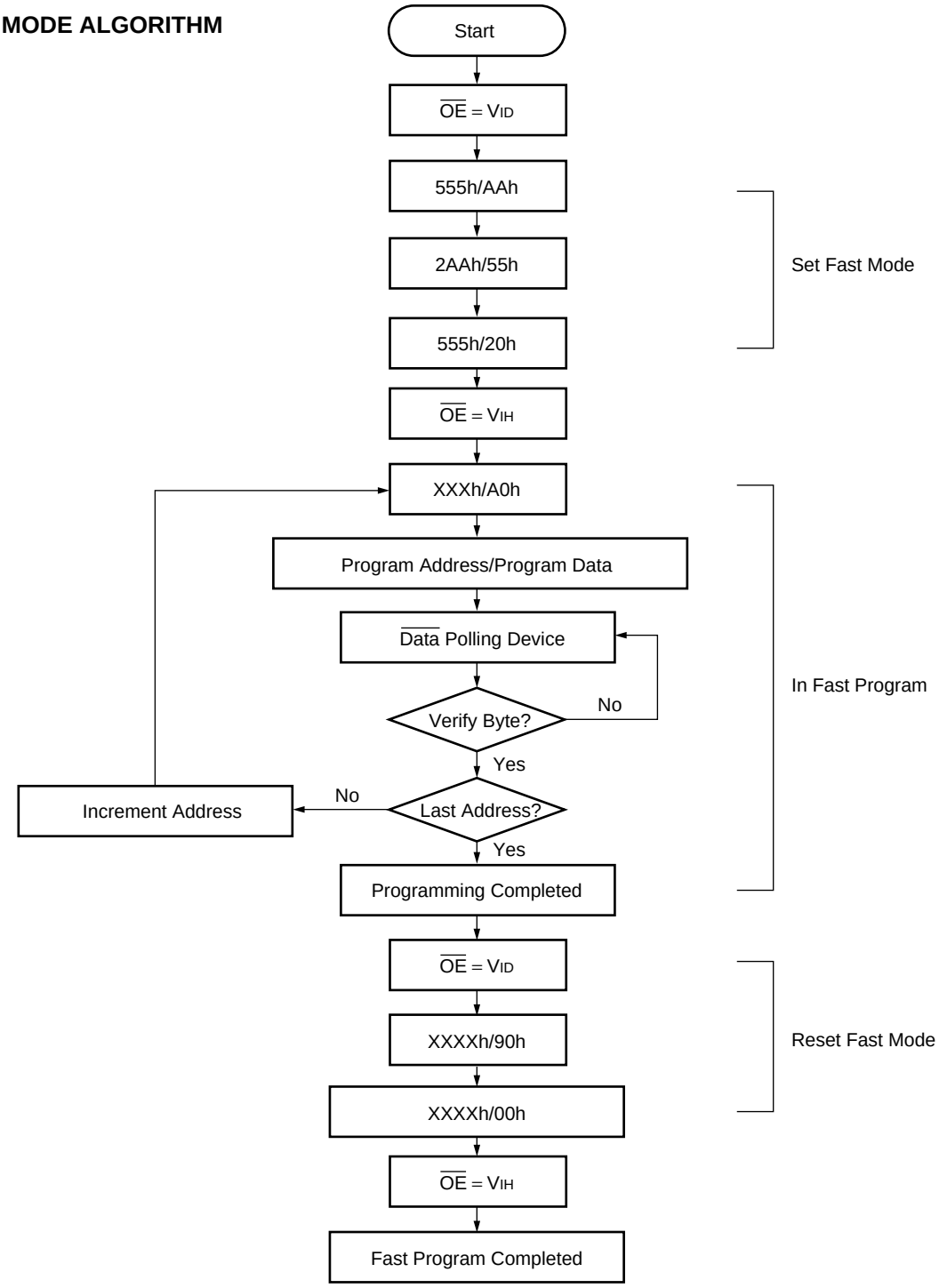
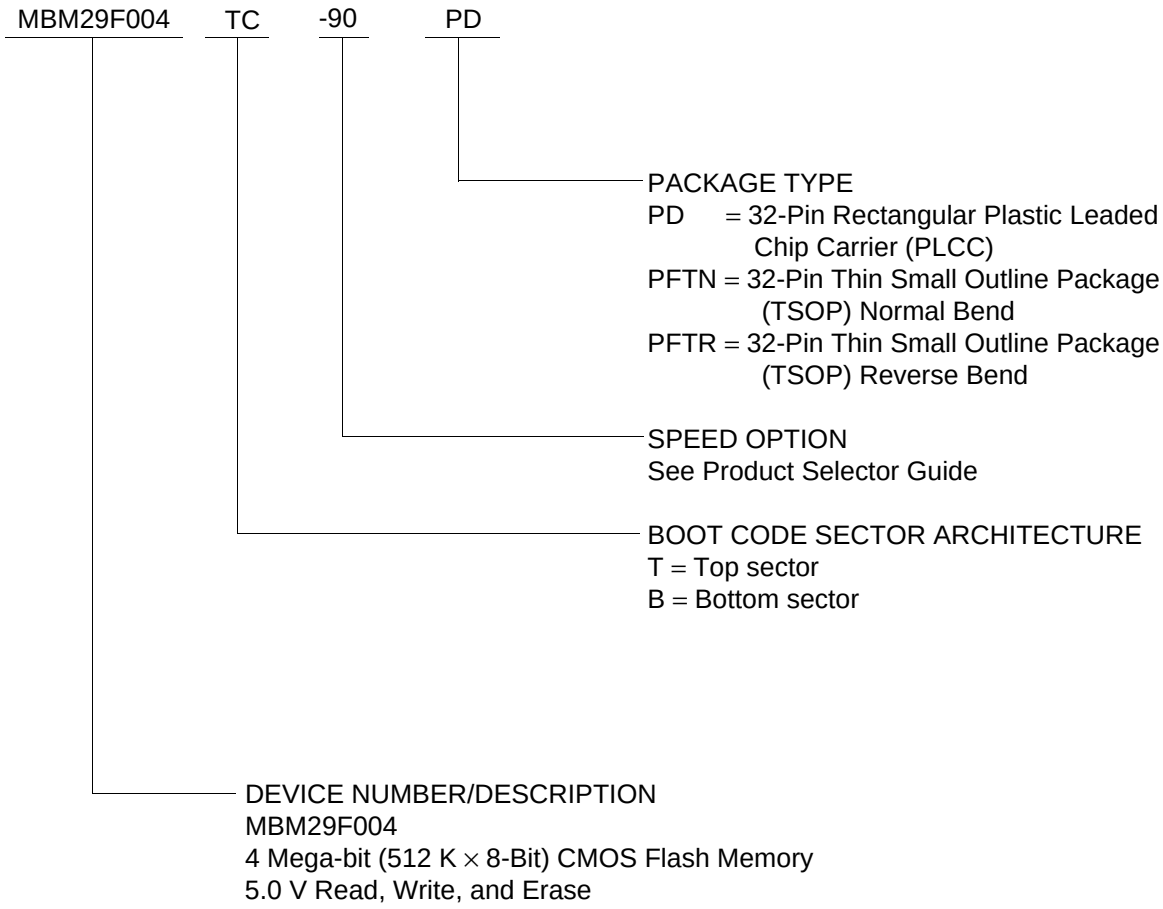


Figure 24 Embedded Program™ Algorithm for Fast Mode

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of :



Valid Combinations	
MBM29F004TC-70 MBM29F004TC-90	PFTN PFTR PD
MBM29F004BC-70 MBM29F004BC-90	

Valid Combinations

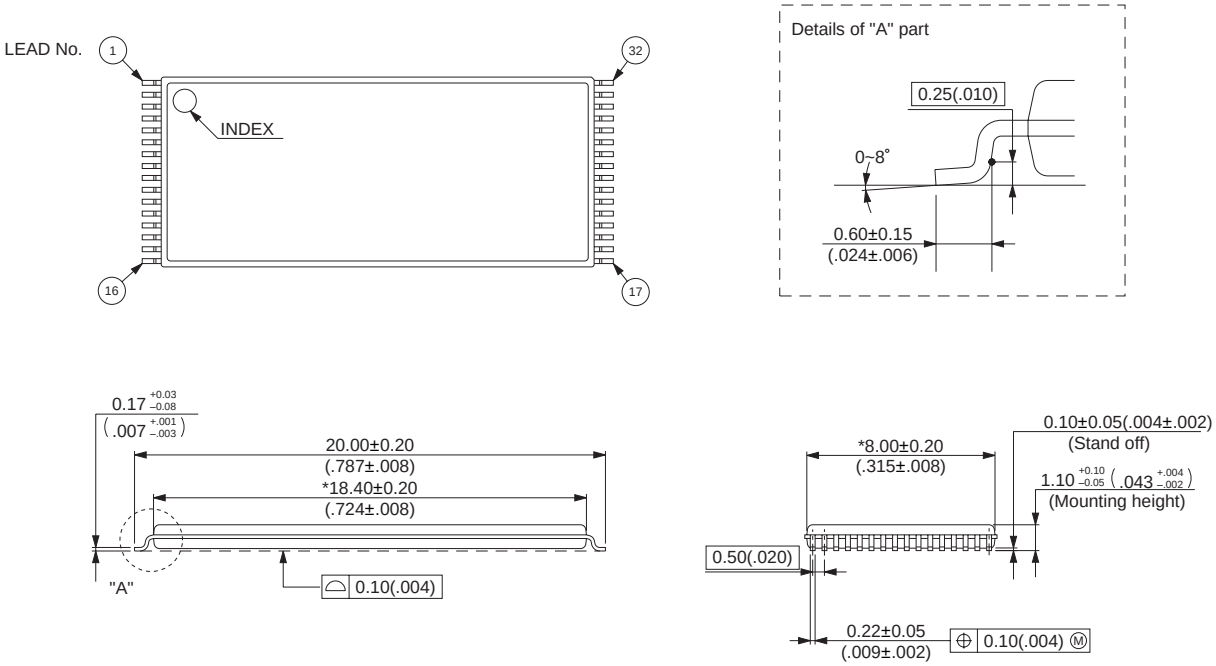
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Fujitsu sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Part No.	Package	Access (ns)	
MBM29F004TC-70PFTN MBM29F004TC-90PFTN	32-pin plastic TSOP (1) (FPT-32P-M24) (Normal Bend)	70 90	Top Sector
MBM29F004TC-70PFTR MBM29F004TC-90PFTR	32-pin plastic TSOP (1) (FPT-32P-M25) (Reverse Bend)	70 90	
MBM29F004TC-70PD MBM29F004TC-90PD	32-pin plastic QFJ (PLCC) (LCC-32P-M02)	70 90	
MBM29F004BC-70PFTN MBM29F004BC-90PFTN	32-pin plastic TSOP (1) (FPT-32P-M24) (Normal Bend)	70 90	Bottom Sector
MBM29F004BC-70PFTR MBM29F004BC-90PFTR	32-pin plastic TSOP (1) (FPT-32P-M25) (Reverse Bend)	70 90	
MBM29F004BC-70PD MBM29F004BC-90PD	32-pin plastic QFJ (PLCC) (LCC-32P-M02)	70 90	

■ PACKAGE DIMENSIONS

32-pin plastic TSOP (1)
(FPT-32P-M24)

Note 1) * : Resn protrusion. (Each side : +0.15 (.006) Max).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



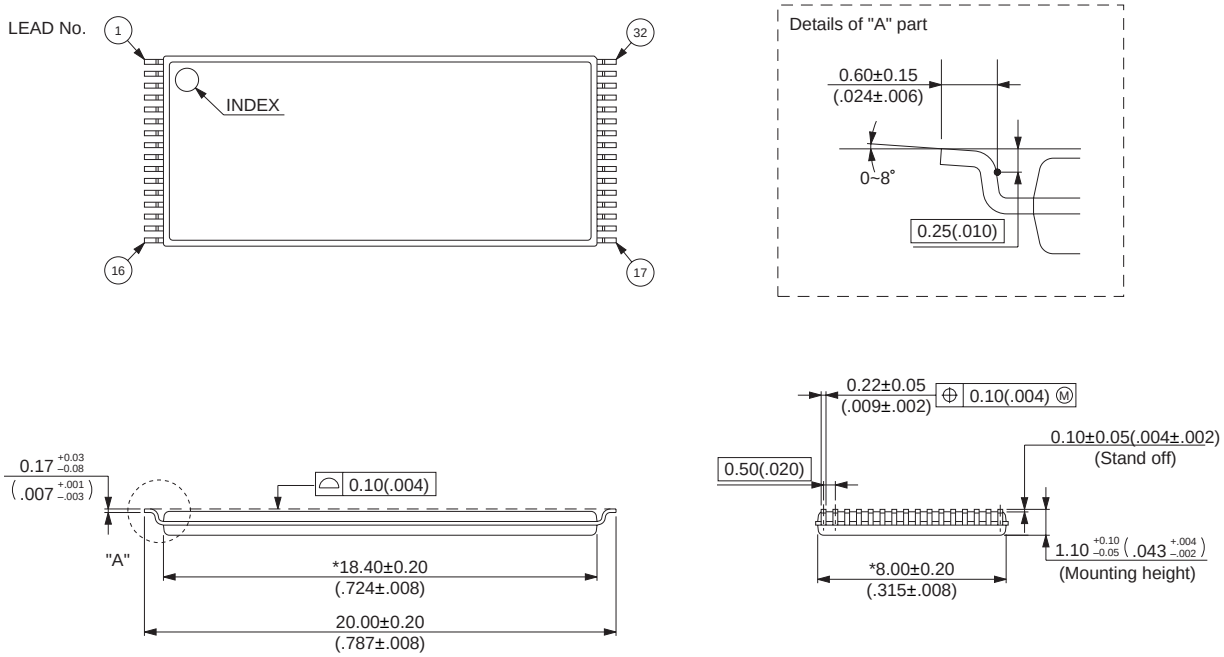
Dimensions in mm (inches)

(Continued)

(Continued)

32-pin plastic TSOP (1)
(FPT-32P-M25)

Note 1) * : Resn protrusion. (Each side : +0.15 (.006) Max).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

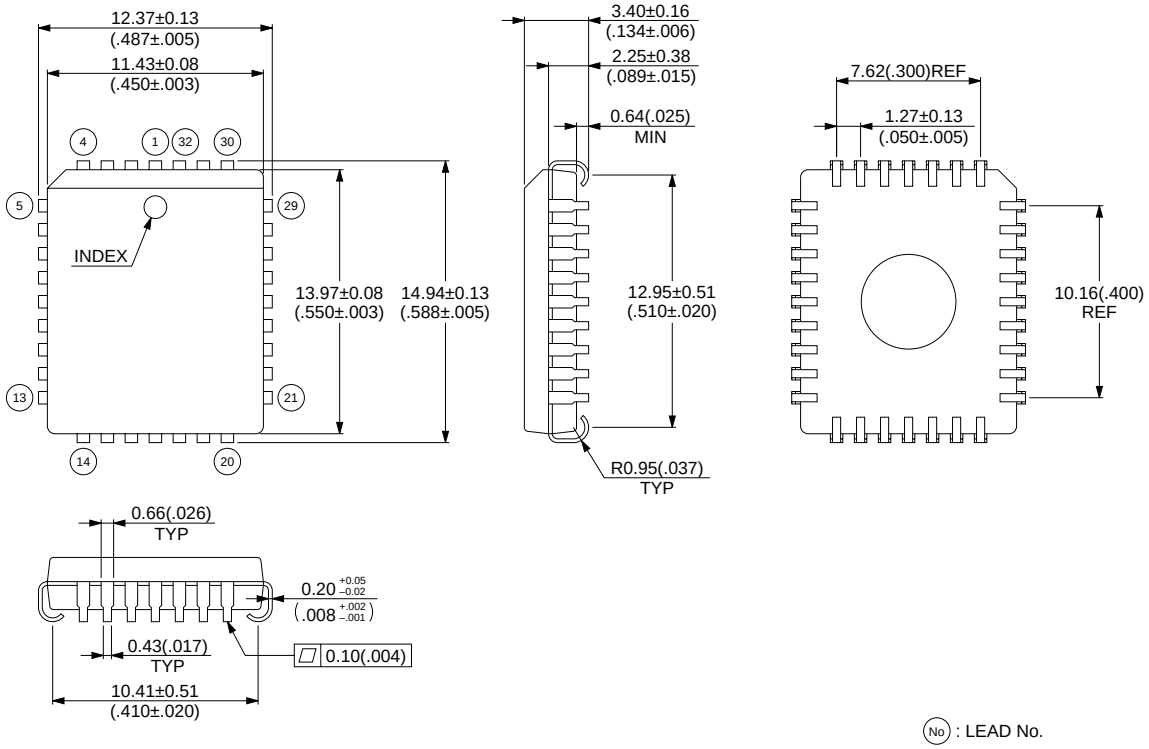


Dimensions in mm (inches)

(Continued)

(Continued)

32-pin plastic QFJ (PLCC)
(LCC-32P-M02)



No : LEAD No.

Dimensions in mm (inches)

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